# MEMS Integration for a Range of Tire Pressure Devices
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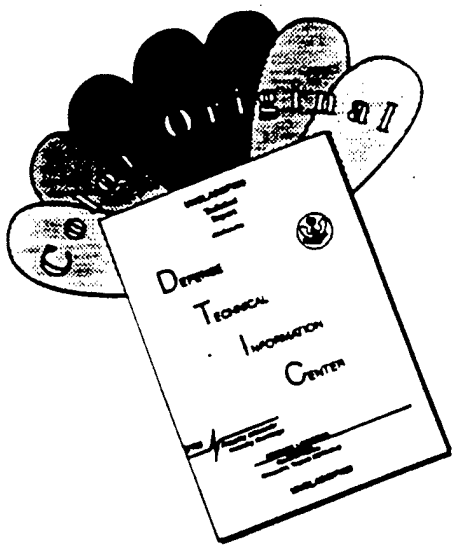


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# ABSTRACT

**This project, Micro Electromechanical System (MEMS) Integration for a Range of Tire Pressure Devices, investigates the feasibility of an innovative design for a retrofittable tire pressure measuring sensor integrated circuit and packaging. The device when developed and marketed will allow consumers and commercial transportation users to easily and effortlessly determine when to reinflate their tires. The projected savings in energy costs and reduction in air pollutants generated are 2% to 8% per vehicle. With approximately 150 million North American vehicles and an equal number in Japan and Europe, the commercial potential and air quality benefit can be tremendous. The feasibility study investigated passenger car, truck, and aircraft tire applications. The project reported on designs and analytical results obtained in studies of corner compensation for anisotropic etch with KOH, surface micro machined capacitor sensing mechanisms, and charge redistribution CMOS analog processing. The designs investigated a subminiature pressure transducer package which provides a unique interface between sensor and tire. Finite element modeling results of the package and MEMS integrated circuit revealed a robust structural design. Spice simulation of the analog circuit showed acceptable performance. The report also identifies key work to be accomplished in order to complete development. Further development was recommended.**

# Acknowledgments

**RainTree Technology acknowledges several individuals who provided valuable technical assistance. Mr. Ed Derian, an independent consultant, provided Finite Element Modeling of the package and MEMS chip mounting geometry. Dr. Selden Crary of Michigan Microsensor, Inc. and the University of Michigan reviewed designs and provided helpful comments. Dr. Kris Pister of UCLA provided help through his MEMS short course and provided additional advisory design review.**

# Table of Contents

# Figures

# Tables

# CHAPTER 1

## FINAL TECHNICAL REPORT SUMMARY

# 1 Summary

This final technical report by RainTree Technology details work progress and findings on SBIR contract #DAAH01-96-C-R037 during the contract period of January 22 to August 22, 1996. The contract objective and title is MEMS Integration for a Range of Tire Pressure Devices.

## *Purpose and Scope*

The study investigated the feasibility of a new tire pressure measurement device. The Sure✔™ device involves a unique miniature package which is a retrofit for tire valve cores Figure 1.1. Because of the small size and packaging constraints, silicon anisotropic etching is a key element of obtaining the desired outline dimensions of the MEMS IC. Also, because the valve core package is miniature, single chip integration of a micromachined pressure transducer with analog and digital circuits is a requirement. The basis of integration study is a 2.0 μm CMOS process. The integration study scope expanded upon finding good feasible potential and high merits of capacitive sensing as well as piezoresistive pressure sensing.

## *Methods, Assumptions, and Procedures*

The investigative approach involved pre-design studies, conceptual design creation, design analysis, and simulations. Prototype design, fabrication, and test, also planned, has been only partially completed. However, the study maintained multiple alternatives with an objective to improving performance while keeping risk low. Thus, for example, the analysis of analog electronic integration focused on a more complicated design for the capacitive sensor than for piezoresistive. In the same vein, the design of prototype items included both simple and more complex options as well as process diagnostic tests. Two experimental designs are complete and ready for near-term fabrication and test. The experimental items support (1) investigation of alternative anisotropic etching masks, (2) design alternatives for implementing MEMS surface micromachining of completed CMOS wafers, and (3) verification of electronic and mechanical computer simulation/analysis.

## *Results and Discussion*

RainTree Technology completed review of tire pressure applications and defined the design specification for the Sure✔™ tire pressure measuring valve core. When manufacturers rejected a (seemingly) simple design for deep draw and metal stamping operations, the critical metal barrel, which is the integrated circuit package, became much more complex than originally envisioned. Several designs and redesigns were necessary to achieve a workable one and a manufacturing process. The impact of the initial design being rejected by manufacturers caused significant delay in completing all of the planned project tasks. However, new designs for the alternative swiss screw machining process proved viable. Fabrication of the new barrel design will enable the planned tests on packaging to proceed. The IC outline dimensions are tightly coupled to the barrel design. Consequently, the initial masks for anisotropic etch "sculpting" of the IC form were revised in concert with the final barrel design.

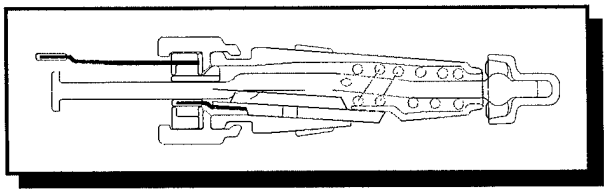

**Figure 1.1** Valve Core Replacement w/ MEMS IC Pressure Sensor — Task Objective

Again, the designs include alternative simple and complex patterns of corner compensation. Because of the small surface dimensions and deep etching, prior corner compensation methods required modification. The degree of success of

these modifications will determine the final circuit layout constraints (e.g., how close the pressure port can be placed to the chip end).

We developed several detailed conceptual designs to support tradeoffs between piezoresistive and capacitive pressure sensing mechanism implementations. These conceptual designs each are based upon using the N-well of the CMOS process as a pressure sensitive diaphragm, Figure 1.2. Although, the piezoresistor may be easier to develop, there are significant advantages of capacitive pressure sensing mechanisms. New isotropic etch processes such as $XeF_2$ have proven to be successful post-CMOS processes to release MEMS surface structures. Although, this too involved significant efforts, parallel designs of competing approaches prevents premature selection of either approach until relative merits and difficulties of each are further evaluated. Factors, including learning curves for L-Edit, TSPICE and other new software tools, increased the work but better equip RainTree Technology for future projects.

Significant analog design work showed the feasibility of meeting design objectives in a 2.0 µm CMOS process. The design basis was a library of analog macro cells but modifications and new circuits were found necessary to achieve acceptable performance. The study produced a simulation of charge redistribution which shows good performance of analog to digital conversion. The completed analog designs provide a starting point for future integration. Testing of integrated circuits of this design will provide validation/correction of the simulation work.

The study for digital circuits identified candidate electronic designs centered around licensable digital processor cores or an early primitive DSP design by the principal investigator. Each design provides necessary processing capability for either piezoresistive or capacitive sensor. Tradeoffs between them are complexity, silicon real estate used, level of maturity of CMOS implementation, and design cost/risk.

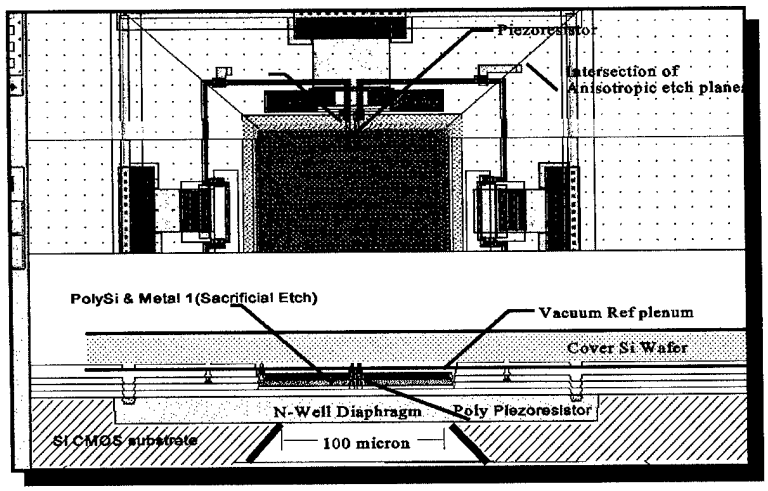


**Figure 1.2** N-well Diaphragm Piezoresistor Design

Finite element analysis results proved the barrel and IC package feasible but underscored the need for test and evaluation over the environmental range of the device. The issue is in the bonding strength of the chip and package.

### *Conclusions and Recommendations*

Concluding remarks in the report discuss the significance of the work and conclude that the basic design is feasible. The risks inherent with incomplete testing are low because there are many feasible approaches which differ mostly in performance. This in turn will determine whether a single device design or variations are required.

The report recommends continuing the development work and further addressing the issues and tradeoffs raised in this project.

# CHAPTER 2

## INTRODUCTION, PURPOSE, and SCOPE

# 2 INTRODUCTION, PURPOSE AND SCOPE

## 2.1 Contract purpose/objective overview

The commercialization potential of this SBIR project derives from the current difficulty and nuisance of regular tire pressure checking. The situation is such that, in all likelihood, the majority of cars and other vehicles operate with tire conditions slightly outside tire manufacturers' recommendations. The exceptions to this case occur at high maintenance costs. For example, the universal world-wide recommendation is that all aircraft tires be pressured checked daily (a significant expenditure of labor hours).

Maintenance of correct air pressure in a tire is vital to the life of the tire and safety of its vehicle (Brady,'82). Tires which are improperly inflated have potential for increased rate of wear and/or increased probability of tire failure. However, there is a no-win trade-off between inefficient, periodic gauging of vehicular tire pressure on one hand and "hopeful neglect" on the other hand. In the neglect mode, drivers hope that pressure stays "acceptable" so as not to significantly increase tire wear or gas costs. Drivers wishfully believe that significant problems will be detected by their observation or their mechanic's routine service checks. This condition prevails in the general personal auto domain because, presently, there is only one practical way to determine the inflation condition of tires. Someone must manually measure the tire interior pressure one wheel at a time while stooped-over or on hands and knees. That is best done while the tires are cold - but that's not the usual time when the opportunity and air pressure are available. It's such a nuisance that even the best of us lean toward a neglect mode. This is an unfortunate fact in spite of the millions of inexpensive manual tire gauges carried in auto glove boxes around the world.

Having other concerns, commercial trucking, aircraft fleets, and the military are generally more disciplined in their tire maintenance procedures. They may even consider temperature and load when evaluating whether measured pressure lies in an acceptable pressure range (Brunot,'83, Schuring,'83). However, realize that businesses whose concerns for safety and cost of operation necessitate properly maintained tire pressure are only taking the best of two bad propositions with planned maintenance intervals for pressure checks. Sufficiently frequent intervals will increase labor hours and costs related to these scheduled checks. Studies by the Alberta Department of Energy show that even in the best maintained commercial fleets there is potential for 2% to 8% fuel reduction savings resulting from correcting improperly inflated tires (MacLean,'92). Therefore, whether private, commercial, or public sector is involved the present status of tire pressure measuring devices leads to increased cost in one way or another. It also leads to higher air pollution (San Diego County,'93). Previous attempts at tire pressure devices on vehicles (Achterholt,'89,'91, Huang,'88, Ichihara,'79, Scheller, '86) have not been commercially successful (Consumer Reports,'93).

The key discriminator of the innovation behind the SBIR research versus the numerous existing implementations of pressure sensors is in the focus of this design towards a retrofittable device. We have found that the valve core is uniquely a common element in all tire and wheel designs. This allows a single basic design of a product to retrofit into all tire markets. The concept being researched is unique in that it fits broad breadth markets with a low-cost retrofittable product. Being retrofittable means that the device can be installed on in-service tires at any

time. The device is suitable for a broad range of wholesale and retail market distribution strategies because of this retrofit capability.

## 2.2 Scope of Investigation

The objectives of the phase I research supported evaluation of the feasibility of this approach and development of advanced designs suitable for full scale development. In our study, we performed the following efforts:

(1) updated and analyzed tire pressure measurement requirements;
(2) developed a MEMS sensor design and sculpted shape in conjunction with design of mechanical package;
(3) analyzed processing requirements and investigated candidate ASIC process and foundry;
(4) simulated sensor signal processing related to several optional signal processing approaches and evaluated the merits and negative factors of each and;
(5) designed test chips to evaluate fabrication steps and sensor/circuit concepts.

## 2.3 Report Overview/Narrative Outline.

This report provides a description of the design and investigation procedures, then discusses the significant results of the investigations. The methods that are significant are design calculations, mechanical and electronic simulations, and experiments. Chapter 3 presents descriptions of the methodologies employed and the assumptions that were made in our analyses. Where appropriate, there are a significant number of references to the relevant prior work of other researchers.

Following initial studies and calculations, we developed several alternative design approaches with respect to each of several specialty areas. From analyses of these designs (employing the methodologies of Chapter 3) we obtained various results and data. Chapter 4 reports on these results by specialty area and design type. Each subsection of Chapter 4 first presents concise descriptions of the options available and the alternatives chosen for design. Text and graphics identify particular features of the designs which relate to the elements discussed in methodology or results. Chapters 3 and 4 also identify the plans for implementing an integrated circuit test chip. Completion of design, simulation, and fabrication of this chip took more time than was available in this phase of the project. Work is incomplete with respect to the test chip evaluations. However, the anticipated experimental evaluation and test plan is described in Chapter 3 and design in Chapter 4. Chapter 4 also discusses findings relative to market status and potential for commercialization of tire pressure measurement devices.

Interpretation of the factual results as related to the feasibility of implementing the project follow in Chapter 5. Risk factors and particularly those that stem from incomplete experiments on the test chip are evaluated. Separate subsections of Concluding Remarks clearly distinguish the interpretations supported by results from hypotheses projected from incomplete experiments. With regard to the latter, much of the interpretation focuses on perceived risks and mitigation strategies. The key results which form the basis of recommendations are identified.

Chapter 6 provides our recommendations with a conditional option. The recommended action plan follows from a low-risk approach with sound mitigation strategies. The conditional option, which modifies specific elements in the recommendation, executes a mitigation strategy if later results are not as expected. However,

validation of expected results will cancel the mitigation actions and eliminate the optioned tasks. The evaluators will find that the recommendation is favorable to the feasibility of further pressure sensor development, irregardless of the conditional results.

# CHAPTER 3

# METHODS, ASSUMPTIONS, and PROCEDURES

# 3 Methods, Assumptions, and Procedures

This chapter presents in detail the research steps and activities conducted relative to the initial design shown below. An extensive literature search provided important data and suggested design concepts based upon prior experimental success. Conceptual designs involving both piezoresistive sensor and capacitive sensing mechanisms were created. Trade offs of alternative design approaches lead to selection of the candidates presented in Chapter 4. Analysis methods of designs included calculation of basic parameters, mechanical design analysis via finite element analysis (FEA), and circuit simulation via Spice electrical analysis.

## 3.1 Design Requirements Assumptions

Briefly the SURE✔™ invention (Widner,'95) is comprised of a valve/transducer and system for pressure measurement. In it, the valve/ transducer is an appropriately dimensioned tapered barrel of metal (probably Kovar). It has a gasket near the barrel's larger opening and a closable valve at the other end. The SURE✔™ invention uses a monolithically integrated pressure transducer and signal processor and interface. This combined transducer and processor is an integrated silicon circuit contained within the tapered barrel. The SURE✔™ invention further includes wireless transmitter/receiver circuits. An indicator with novel displays of useful tire inflation and maintenance parameters finishes the product.

### 3.1.1 Valve Core Replacement Sensor

Figure 3.1 shows in an exploded view the relationship between a replacement valve core, a stem extending transponder, and a cap. When installed in the stem, the valve core is positioned such that the gasket compresses against the valve core bore surface. It is held in place by a nut engaging the interior threads of the stem. The transponder installs over the outside stem threads and mechanically extends it while electrically connecting to the core. The cap containing battery and energizing circuits installs over the transponder.

#### 3.1.1.1 Valve Core Pressure Sensor and MEMS Integrated Circuit

The following description of the valve core replacement pressure sensor and MEMS integrated circuit overview the design objectives and assumptions that started the research project.

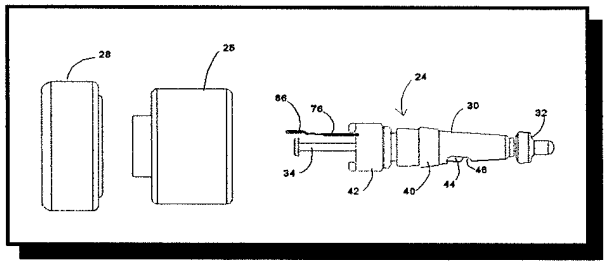


**Figure 3.1** SURE✔™ Components (patent pending)

Figure 3.2 reveals a modified internal physical configuration of the existing valve core. This change provides for additional space within the barrel to mount the pressure transducer IC. As shown, the IC mounts on the flattened inside surface in the barrel. It attaches by means of conventional die mounting adhesive. The adhesive also fills an annular gap between the barrel and the IC as it passes through. This forms a continuous solid barrier which is leak proof within the specifications for the operational pressure ranges expected.

The IC itself will contain an integrated micro-

machined pressure transducer. The transducer consists of a flexible diaphragm and a pressure reference cavity. A set of four piezoresistors are fabricated in the area of peak flexure strain on the transducer diaphragm. The piezo-resistors interconnect in a sensitive bridge circuit which

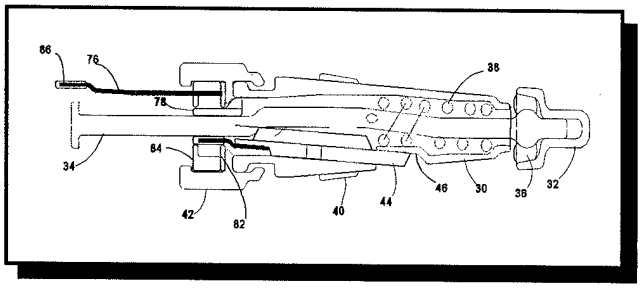


**Figure 3.2** - Cross Section of New Valve Core

provides an electrical signal proportional to a pressure differential applied to the diaphragm.

All parts of the design are capable of very economical mass production. Example construction processes are:

(1) Swiss screw machine milling of a blank followed by die stamping of the blank into a finished barrel and nut;
(2) Metal stamping for cup and pin;
(3) Plastic injection molding for guides and retainers; and
(4) Printed circuit fabrication.

Of course, the MEMS processing and conventional integrated circuit fabrication (for example CMOS fabrication processes) are highly supportive of mass production. This project's efforts were to develop an initial MEMS design and fabrication plan and to consider the feasibility of its implementation.

The dimensions of the core are determined by a form, fit, function mechanical interface with the TRC 1 valve core bore. This yields approximately 27 mm in length from end of the cup to end of the pin. It is 4.3 mm diameter at the (uncompressed) gasket tapering to 2.7 mm at the smallest diameter of the barrel. The IC chip, Figure 3.3, including minimal encapsulation, must measure approximately 8.9 mm in length by 2.0 mm in width by 1 mm in height. Known piezoresistor (absolute) pressure sensors of similar range, in die form, are approximately 1 $mm^3$. Allowing 1 $mm^2$ area for the sensor leaves the remainder of the chip for integrating high dynamic range analog circuits, analog to digital converters, and a microprocessor with RAM and ROM. These circuits will be implemented in mixed signal commercial 2.0μm or 1.2μm CMOS (Orbit,'96, Foresight,'96, Mosis,'96). The microprocessor can be implemented from licensed VHDL synthesis of a proven large volume production microprocessor (Pine DSP,'96, Western Design 6502,'96, Vautomation,'96, Bier,'95) supported by C+ software tool sets.

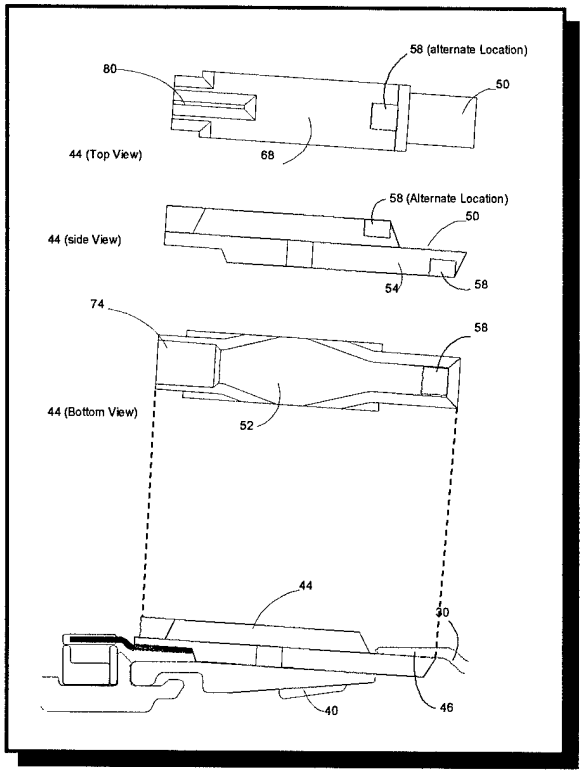


**Figure 3.3** - MEMS Integrated Circuit

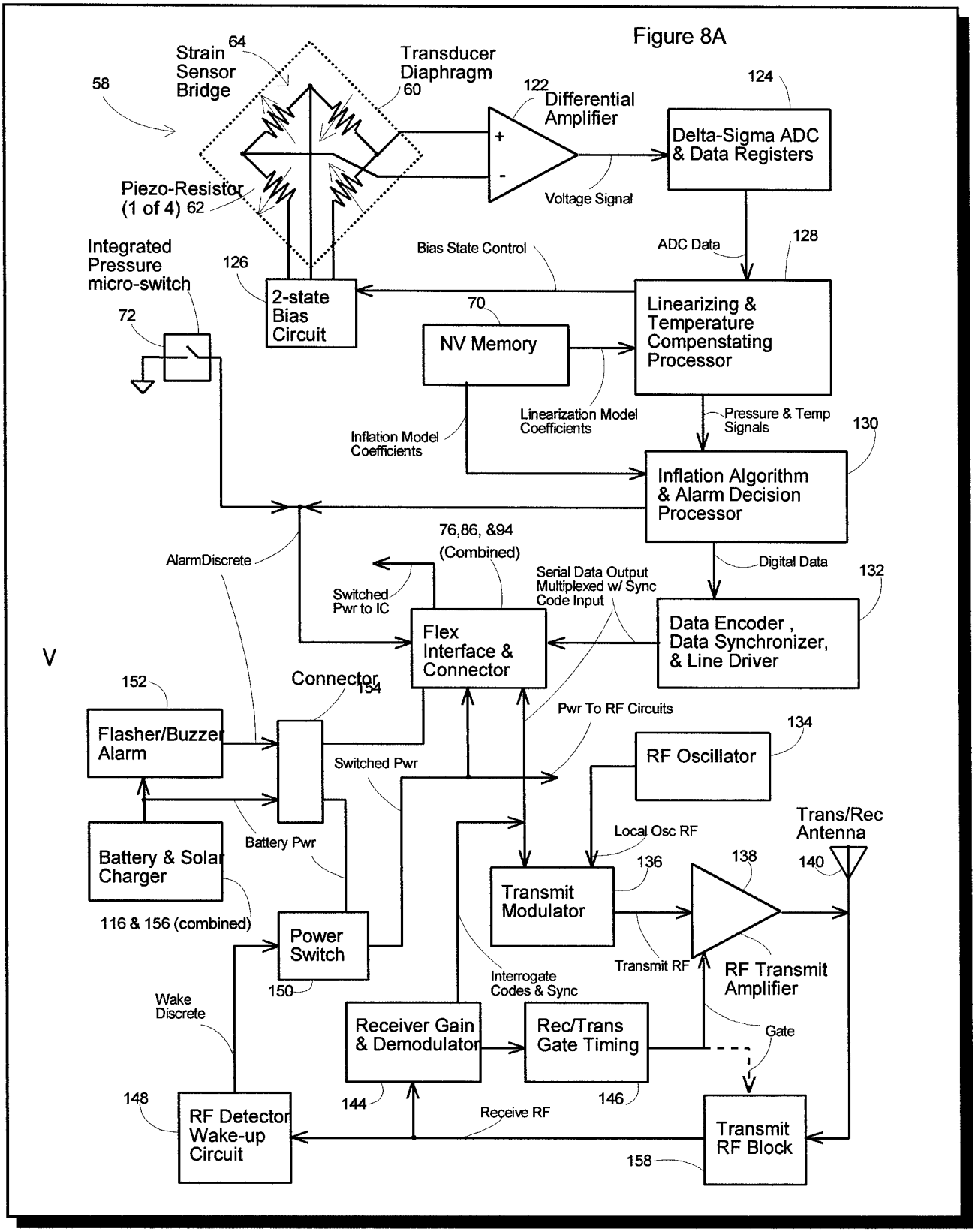


**Figure 3.4** Notional Sensor/Transponder Block Diagram—MEMS Integration Upper Half to Flex

Table 3.1 - **Design Parameters**

| **Function or Parameter** | **Requirement** | **Impact or Tradeoffs** |
|---|---|---|
| Sensor type (gauge, absolute) | gauge desirable, absolute acceptable | Gauge design more complex; environmental factors and safety issues exacerbated |
| Pressure range (all applications) | 4psi to 350psi gauge pressure (applications within range form essentially continuum vs separated range bands) | Single design with high dynamic range or multiple design variants |
| Pressure range (largest range for single tire use) | 8psi to 120psi (military truck with off road and paved road utility adjustment in pressure) | Defines absolute minimum dynamic range of pressure sensitivity |
| Form factor | Two standard valve core sizes fit 100% of applications - large valve core applies to very few applications | Maximum of two physical configurations needed - potential for a single MEMS IC design if high sensitivity and wide dynamic range |
| Pressure accuracy | error less than 1psi (independent of pressure value) | Output signal minimum 12bit accuracy (if full scale spans pressure range); input signal needs higher resolution if 0psi signal offset from 0 volts |
| Temperature environment | -55°C to +85°C full performance. To +160°C degraded performance and survivability | Wide temp span signal processing and temp compensation of sensor |
| Sensor implementation | Piezoresistive | Established; simpler design; limited responsivity/ sensitivity laser trimming frequently used for device calibration |
| | Capacitive | Surface micro machining and anisotropic etchnig required; wider dynamic range due to higher responsivity & sensitivity |
| | optical, tunneling, thermal | design issues |
| Self-test, recalibra-tion in use | User inputs - high priority goals | Add actuator to system for self-test feedback |
| Media environment | Aircraft - dry $N_2$;<br>Commercial - dirty air, moisture, compressor oils;<br>Heavy equipment ( water ballast) - $H_2O$ saturated air probable sensor immersion in water and/or oil films;<br>All - partial pressures of out gassed hydrocarbons, rubber dust and particulates | Design constraint: isolate electronic circuits from media, passivate |
| Power consumption | Rechargeable battery voltages; micro power circuits with power down and standby modes of power reduction | Limitations in sensor implementation; lower operating voltages, bias currents, actuator forces |

| Function or Parameter | Requirement | Impact or Tradeoffs |
|---|---|---|
| Silicon processing | Compatibility with existing foundry processes | CMOS compatible designs; thin films not optimized for surface micro machining |
| Shock and vibration | Higher ambient compared to ambient for air bag accelerometers, same handling shock specifications | Load factors on released microstructures; stress on chip I/O |
| Centrifugal acceleration | High speed tires subject device to continuous high accelerations of random orientation | Error source in sensor; load factors on released microstructures; stress on chip I/O |
| Non-tire applications with same form factor and size | Air spring in hydraulic or pneumatic shocks/struts | Extremely high (8000psi) operating pressures and worse over pressures |
| | Refrigeration and air conditioning fill valves | Within operating ranges of tires - higher operating temperatures at compressor outlet; Temperature rate of change (temp shock) is high |

Table 3.1- **Design Parameters (continued)**

### *3.1.1.2 Transponder and Valve Cap Electronics Assembly*

The transponder wireless electronics is not an issue of the research of this report. There is a wide number of new designs and commercial miniature integrated circuits in the wireless technology area. The applications relative to this product primarily center around the class of devices for wireless RFID assemblies. These and other miniature wireless systems have been demonstrated (Kaiser,'96,Obrist,'95, Yamagishi, '95). The assumption made is that designs in this technology will be available for inclusion in the SURE✔ system. A notional block diagram of the system is shown in Figure 3.4 for reference. Requirements and issues of MEMS investigation center on the upper half of the block diagram.

The design constraints for this concept of tire pressure measurement prove to be very challenging. Table 3.1 identifies the parameters which are important to the design of the tire pressure device.

Packaging constraints are also severe. Construction of the pressure sensor elements involves surface micromachining and anisotropic bulk etching. The valve core dimensions lead to custom packaging and an IC form factor (Figure 3.3) not typical of present electronic and MEMS components. There is no choice between two chip and single chip designs (e.g. that were available to commercial accelerometer and larger pressure sensor products). A single long, thin chip, with I/O connections situated at one end is dictated by these constraints. Conventional wire bonding is also not an acceptable means of interconnecting the chip die to the device I/O.

## *3.2 Research Approaches / Methodology*

MEMS pressure sensors are well known. They were early successes in MEMS technology (Petersen,'82, Diem,'95). Our approach was to implement a new design - none existing fit the valve core form factor. However, within the new design, it was desired to build upon proven

techniques of which there are many. In addition to pieozoresistor based sensors (Akbar,'92, Dziuban,'94, Gukel,'91, Marco,'93, Mosser,'91, Schellin,'95), many other physical means of sensing pressure are available. Capacitive sensors are well known in experimental work (Artyomov,'91, Habibi,'95, Kudoh,'91, Kung,'92, Nagata,'92, Pons,'93). Pressure variable tension of mechanically resonant strings and beams has been employed for sensing (Bartelt,'93, Bogdanova,'93). Capacitive and optical (Angelidis,'92, Bartelt,'93, Kim,'95) excitation/sensing of the sensing mechanism have also been employed. Closed loop feedback circuits with sensors have provided the highest sensitivity and accuracy in sensors of all types (Kaiser,'94, Kemp,'95, Kromer,'95, Weijie,'92). Candidate designs for this project considered trade offs in the techniques above.

### 3.2.1 Design Analysis and Simulations

Properties of silicon and semiconductor films drive the selection of the final design. The prior work in characterizing these properties, particularly those which provide analytical equations for the results, was important. For example, Guckel ('91) and Biebl ('95) provided important equations and material properties for the analysis and selection of design parameters of sensor diaphragms. UCLA's MEMS short course (Feb '96) provided useful analysis techniques and process evaluations.

#### 3.2.1.2 Mechanica FEA

The mechanical properties of the silicon integrated circuit and the unique valve core package are extremely important. The chip, package, and interface between them are subjected to loads resulting from pressure and temperature. Finite element modeling using commercial software (Pro/Mechanica) was used. Material properties from Petersen ('82) and Reichl ('91) were the basis for silicon and adhesive parameters used in the simulation (see Appendix A).

#### 3.2.1.3 Electronic Circuit Design

The requirement is an integrated MEMS sensor chip consisting of three types of circuits (see Figure 3.4):

(1) pressure sensitive circuits consisting of a MEMS structure and interfaces;
(2) analog circuits to interface with the sensor, perform sensor output signal conditioning, provide sensor conversion/signal processing and power conditioning; and
(3) digital circuits to perform control of the sensor, process the sensor output, and execute I/O control.

Reported electronic designs of interest and value to this design comprised mostly capacitive sensing and/or feedback actuator control as above. Design analysis and descriptions of electronic circuits from MCNC ASIC (MCNC,'96), and accelerometer technology (Boser,'95, Kemp,'95, Kromer,'95, Weijie,'92) were useful. Capacitor sensors from Jordan ('91), Kung ('92), Schnatz ('92), and UCLA short course materials provided a basis for sensor processing employed in the capacitive readout circuits reported in Chapter 4. Evaluation of circuit designs was by simulation using T-Spice from the Tanner Pro software. Models, CMOS analog cells, and circuit examples from Tanner Pro software library assisted design significantly. Model parameters were updated as necessary from MOSIS monitor circuit test data.

### 3.2.2 MEMS Experiments

Two experiments in fabrication of MEMS integrated circuits were planned to verify analytical and simulation results. The first investigates anisotropic etching to "sculpt" the unique form factor of the sensor IC. A successful result provides "dummy" silicon IC chips (obtained by corner compensated bulk micromachining of a blank wafer). Installation of these into fabricated barrels allows test of the sensor packaging concept.

A second experiment's objective was to verify the design of candidate sensor structures on an integrated circuit test chip. The experiment evaluates:

(1) candidate MEMS pressure sensor designs and validate prototype sensor design assumptions;
(2) suitability of established MEMS processes for post CMOS processing to complete sensor fabrication; and
(3) signal responses and compare them with simulation results.

### 3.3 Noteworthy information/ Assumptions

In summary of substantive information derived from noteworthy trips, meetings, and special conferences held in connection with the contract during the reporting period, there is one significant result. This information was substantiated by two meetings. The critical information from these two meetings significantly impacts current and future research conducted in this project.

The first of these was a private meeting with Dr. Donald Silversmith, Research Analyst of Wayne State University. The meeting occurred in the context of mutual participation in the UCLA MEMS short course. Dr. Silversmith believes that the automotive industry's primary requirement is that sensors have embedded self-test to ensure safety of operation and to mitigate liability issues. The following example of a self test need clearly states an unavoidable requirement. Suppose an individual is injured or killed by over inflating a tire so that it explodes as a result of a failed sensor. A very effective self-test system with a good cautionary display to consumers is mandated.

Another meeting was held with Mr. Scott Stokes, Hill AFB and his engineering group. These product support engineers, responsible for aircraft tires and rims at Hill AFB evaluated past Air Force experience with on-wheel tire pressure devices which led to another requirement of self-test. They stated that past systems have not resulted in reduction of maintenance labor because of calibration issues. Due to mistrust of the system readings, maintenance personnel frequently used conventional gauge sticks to verify the on-wheel system pressure readings. Mr. Stokes identified positive calibration as a top priority for supporting the installation of any system. The C-5 SPD at San Antonio ALC is planning the installation of a mechanical (balloon indicator) system and have requested Hill AFB support. Mr. Stokes' engineers have no confidence in the system accuracy and benefit and so have declined to support it. They also revealed that central integrated tire inflation systems (CITIS) were previously removed from the C-5 and B-1 aircrafts. The systems were ineffective compared to the logistics support requirements and added maintenance caused by the complexity of the system. The engineering team at Hill AFB expressed high interest in this SBIR project and are likely candidates to sponsor PRAM funded project to implement and test this product. Mr. Henry Pollack of Wright Labs also recognized the need for a project of the type and indicated that he would give a proposal priority consideration.

# CHAPTER 4

# RESULTS AND DISCUSSION

# 4 Results and Discussion

Analysis of MEMS anisotropic and isotropic etching along with CMOS fabrication steps led to selecting capacitive and piezoresistor sensing techniques for further design and tradeoffs. Table 4.1 provides a summary comparison of the tradeoffs between these two sensor methods. Given the potential to better fit more of the design requirements (refer to Table 3.1), capacitor sensing is more desirable. But, given the previous commercial success of piezoresistor pressure sensors and the lack of a known commercial capacitor sensor, the piezoresistor approach cannot be ignored.

Because the sensor is highly integrated mechanically and electronically, there are many more very significant issues which influence the final selection. Mechanically the IC form factor and valve core barrel are highly interdependent. Significant problems with regard to the interface slowed the progress of these investigations. But the problems are solved and the results reported in subsection 4.1.

Subsection 4.2 provides detailed reports first on piezoresistor sensors and then capacitor sensor designs. The limits imposed by starting with production CMOS fabrication are seen in subsection 4.2 results. There are significant differences between such a constrained design and the majority of capacitive sensor approaches previously published.

The last two subsections provide electronic circuit designs and findings relative to the commercial market.

## *4.1 Packaging Related Technology and Design*

Initial research verified the form factor and dimensions of the valve core package. It must conform to the interface defined by The Tire and Rim Association, Inc (TRA). In particular, the dimensions and tolerances of Standard Bore Core Chamber No. 1 and Standard Bore Core Chamber No. 3 (1996 Year Book, Tire and Rim Association) apply. Both of these standard bore chambers accept a short core TR C1 valve core which has application in almost all of the configurations identified by the TRA.

| Piezoresistive | Capacitive |
|---|---|
| + High linearity | - Poor linearity |
| ? Good pressure sensitivity (60-80 ppm/Torr) | + 10X better pressure sensitivity (1000 ppm/ Torr) |
| + Easy to fabricate and package | ? Harder to fabricate (sealed lead transfer) |
| + Easy to interface (low output impedance & noise) | - Hard to interface (noisy & susceptible to parasitics) |
| - High temperature sensitivity (1-2 Torr/°C) | + 10X lower temperature sensitivity (<0.05 Torr/°C) |
| - High power dissipation | + Low power dissipation (set by electronics) |
| - Low dynamic range (full scale $\Delta R/R \approx 2\%$) | + High dynamic range (full scale $\Delta C/C \approx 100\%$) |
| -High leakage current in junction isolated resistors | + Potential for self-testing & auto calibration |
| | + Built-in over-range protection |
| -Less scalable: stress averaging limits diaphragm diameter; diffused resistors limit diaphragm thickness. | + More scalable in thickness; diameter limited by absolute value of capacitance |

Table 4.1 - **Piezoresistor vs Capacitance Sensor Tradeoff Summary**

The maximum size IC envelope allowed by the valve core barrel limits design. One choice is

between "flipped" and "non-flipped" orientation of the CMOS circuit. An anodically bonded 'sandwich" comprised of a silicon cover chip o a sensor chip provides four planar surface choices for the CMOS circuit. The best choice for circuit real estate, heat conduction, and implementation of pressure ports and reference plenums is a middle plane of the sandwich. Isolation of the pressure media, mostly dirty air, from the circuits further narrows the choice to the plane shown in Figure 4.1.

Dimensions resulting from finalizing interfaces were less than initially anticipated. The smaller dimensions provided less active area for CMOS gates and set upper limits on the diaphragm size. Extension of the rectangular area of the chip partially compensates as does the <111> plane orientation at 54.7°. Nevertheless, the identified licensable CMOS VHDL cores will fit the available area with custom floor planning.

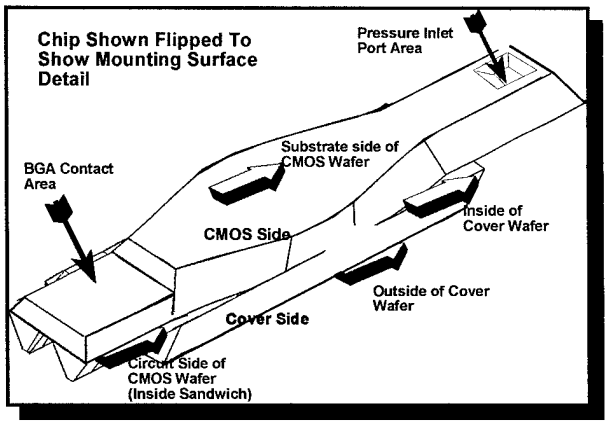


**Figure 4.1** Sensor IC Feature Reference

### *4.1.1 Barrel Design and Fabrication*

Figure 4.2a presents an initial barrel and chip packaging detail with dimensions. Kovar alloy metal was chosen for its low temperature coefficient of expansion approximately matching that of silicon. The drawing was transmitted under proprietary information agreements to several deep drawing (a metal stamping process) and metal casting fabricators for prototype and production quotes. Nearly all objected to Kovar material being used claiming it difficult to work with. However, the internal flat in conjunction with the circular outside cross section was a feature that deep drawing processes are incapable of producing. What was surprising was the length of time for vendors and manufacturer's representatives to relay that feedback to us.

A redesign for screw machining also found manufacturers with that process unable to work with Kovar. However, one vendor has been located who routinely works with Kovar and has screw milling machines dedicated to it. Further design revisions to finalize a screw milling configuration were necessary. These new configurations are now in review for quoting by two vendors.

In order to comprehend the complex three dimensional geometry of the barrel and IC interface, we found it necessary to change from AutoCAD r10 to AutoCAD r13. Revision 13 supports solid modeling. This was an important tool in producing a design suitable for milling rather than drawing. Figure 4.2b shows a solid model simulation of milling operations with standard cutting tools. The 3D wire frame views show how these simple steps can construct the interface between the sensor IC and barrel.

Jeropa Swiss Precision of Escondido is also working with RainTree Technology to ensure that any new design will be transferrable to production. Typical parts in evidence at the Jeropa facility were dental implant posts and very small medical items all near the size and complexity of the barrel. Although Jeropa is ideally suited to fabricate the redesigned barrel parts, unfortunately they began a scheduled three week summer holiday shutdown the next day after our

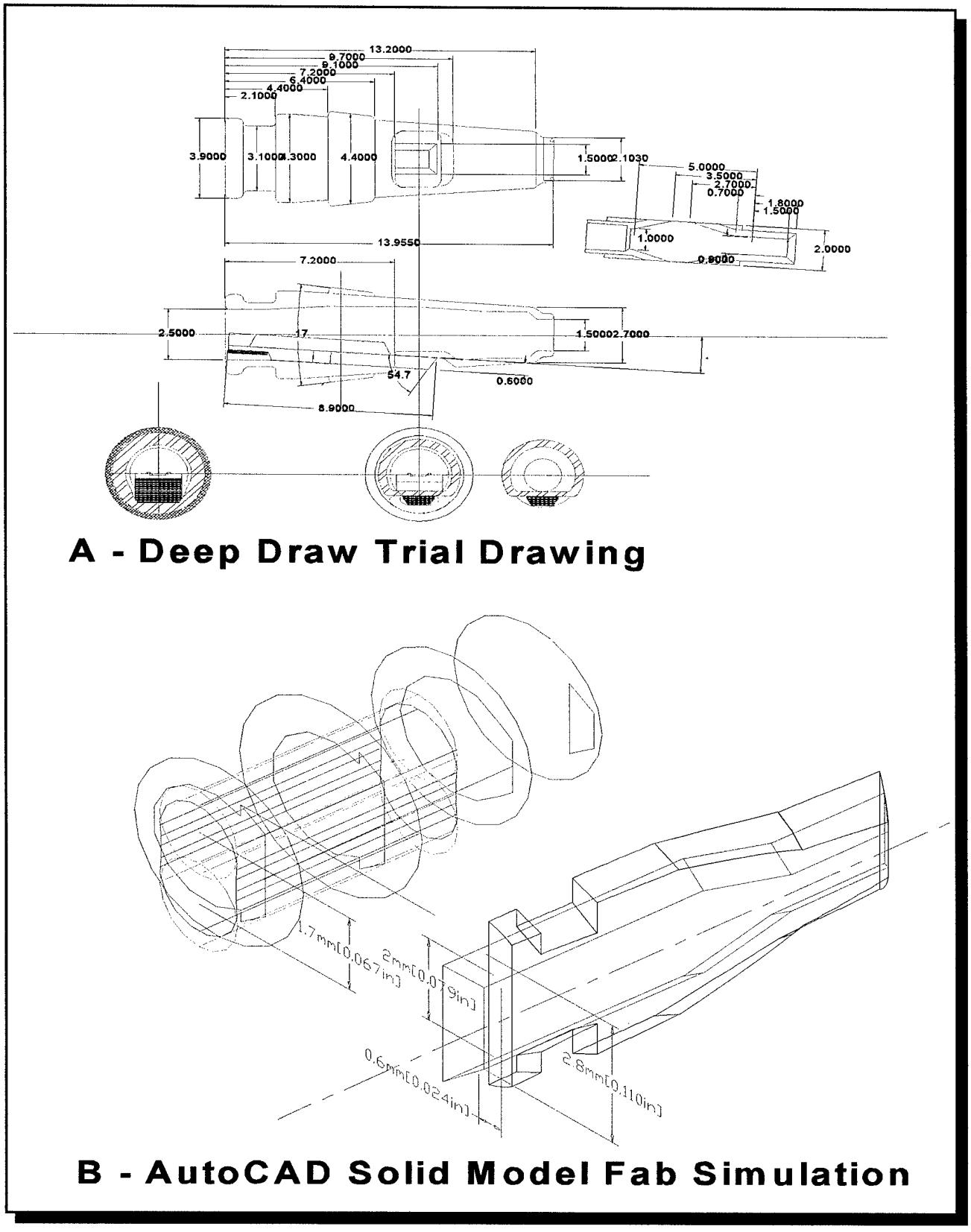


**Figure 4.2** (A) Deep Draw Trial, (B) Simulation of Milling with Cutting Tools (green)

initial contact. That initial meeting was very positive. Their principal technical expert not only thought the design workable, but he also began discussing producibility improvements. The anticipated production fabrication steps using a combination of swiss screw milling and die stamping processes are:

(1) construct slightly oversize blanks by screw milling, and then
(2) die forge the final shape of the internal and external features of the barrel.

Tooling is required for this process, but the combination of processes appears to be the most cost efficient for high volume production.

Initial prototypes for evaluation of bonding characteristics will be completely fabricated by swiss screw milling. Therefore, minor compromises in feature shape and/or thinner walls may be temporarily necessary. But with Jeropa, input we now believe the barrel fabrications problems solved.

On the positive side of this trying experience, we serendipitously discovered another design improvement. The chip outline can be simpler and more rectangular by allowing barrel wall thinning or hole break through in noncritical areas.

### *4.1.2 Anisotropic Milling*

Figure 4.3 presents mask patterns for the anisotropically milling or "sculpting" of the sensor chip outline. The design anticipates double- sided anisotropic etch of a wafer sandwich as shown above. Potential anisotropic milling processes include well known KOH-isopropanol (Barycka,'95,Fjelstan,'96,Offrereins,'91, Zielke,'95) and EDP etching processes (Schnakenberg,'89, MOSIS MEMS guide,'94, UCLA,'96). Both KOH and EDP etch aluminum as well as silicon - a drawback for post processing wafers including CMOS circuits. TMAH etching is a promising etchant which is more selective for silicon. Using TMAH, the aluminum conductors do not require protection. However, the results with TMAH have been highly variable, ranging from very successful to completely failing.

Several anisotropic mask patterns were designed to accommodate 1.0 to 2.0 degree error in mask alignment with the <110> orientations of the silicon substrate. This alignment error limits the number of contiguous patterns in a layout without unacceptable etching-mask undercut.

Approximately 250 devices fit four inch wafer when arranged as a 2x2 cell. Improvements in density were examined with the experimental mask of Figure 4.3. A higher number of devices per wafer may be achieved by changing the arrangement to 3 rows (or more)x2 column cells. This requires either decreasing mask alignment error or achieving good etch mask compensation. The layout shown is indicative of the finished etch prior to dicing and does not show the corner compensated etch mask.

### *4.1.3 Package I/O Pads and Interconnection*

The detail of Figure 4.1 shows interconnection of the IC via solder bump ball grid array (BGA). BGA is a current hot topic in electronics in that it increases the density of interconnections for large pin count IC (FlipChip Technologies,'96, Caruthers,'96,Doane,'93,Fjelstan,'96,Normington ,'95, Reichl,'91). Density and small I/O pad size is important in this design also. The area available for interconnection is small. But more important, wire bonded interconnection is not very feasible. High g loads and vibration are very destructive to wire bonds and a conventional lidded package to protect and seal the leads is not viable.

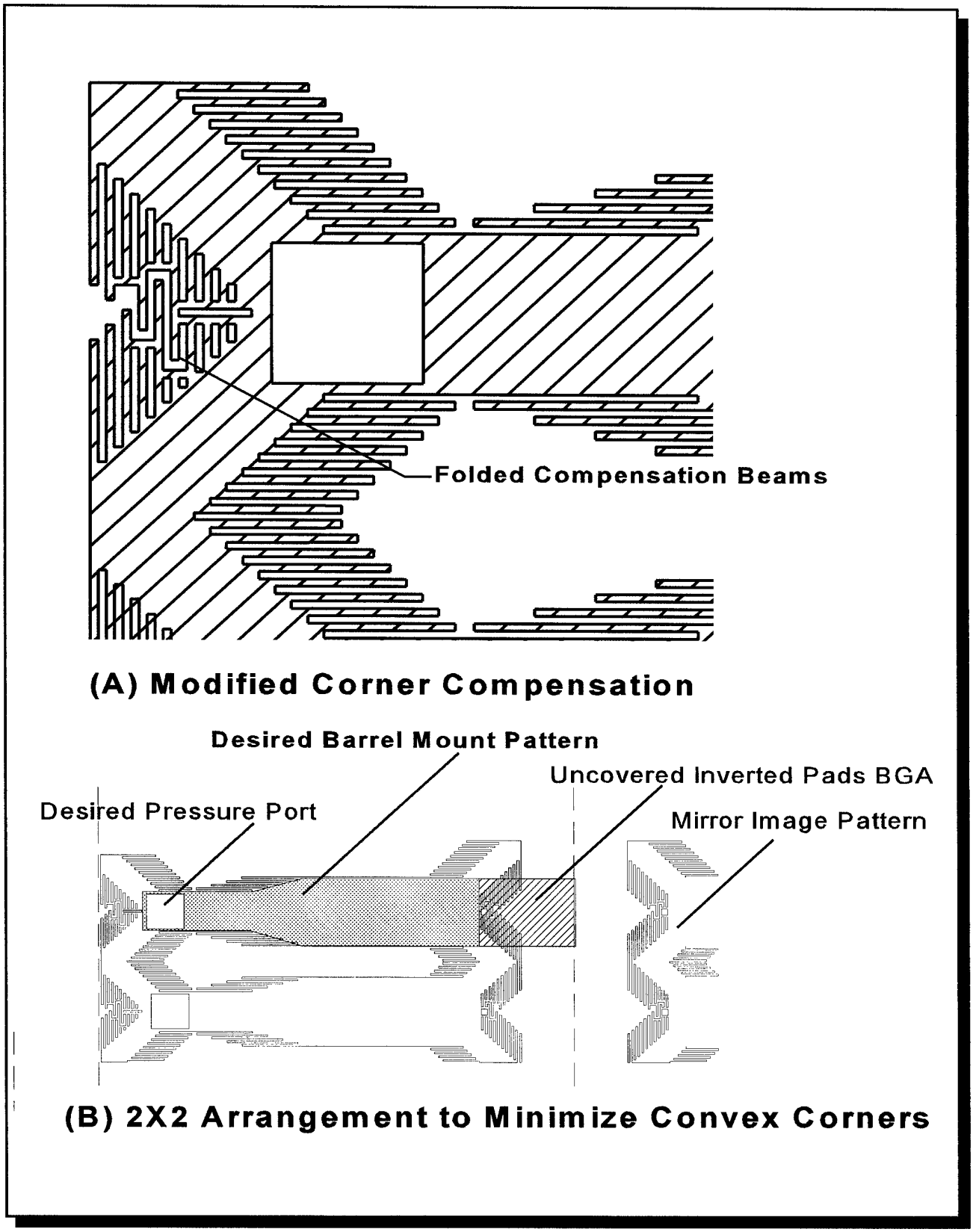


**Figure 4.3** Etch Mask Example (Modification of Offreins, '91)

The anisotropic package sculpting is designed to open inverted pads as shown in Figure 4.1. The bottom (substrate side of metal pads) contacts sacrificial substrate while the top side is covered with oxide layers. The inverted pads connect to nearby normal pads (with circuit protection features). The cover wafer substrate supports the inverted pad after sculpting. Anisotropic etching with TMAH would simplify the uncovering of the inverted pads. The design follows the guidelines published by FlipChip Technologies, but it is not known whether the processing can easily occur at the bottom of the etched trench. Additional investigations are required.

## *4.2 Sensor Related Micromachining Technology and Design*

Sensor construction is very constrained in the selected approach. CMOS processes determine the layers available. The process recipes used to construct the layers are generally proprietary. Design rules from the Orbit CMOS families formed the basis of study of diaphragm and sensor fabrication. Generally the post-CMOS process for all designs in this subsection are as depicted in Figure 4.4 for a piezoresistor sensor design. The following results use only the materials and layers found in the design rules for constructing MEMS diaphragms and capacitor plates. The investigations found that either a 2.0 μm N-well or a 1.2 μm offering from Orbit were viable candidates for construction of a pressure sensitive diaphragm in the location desired.

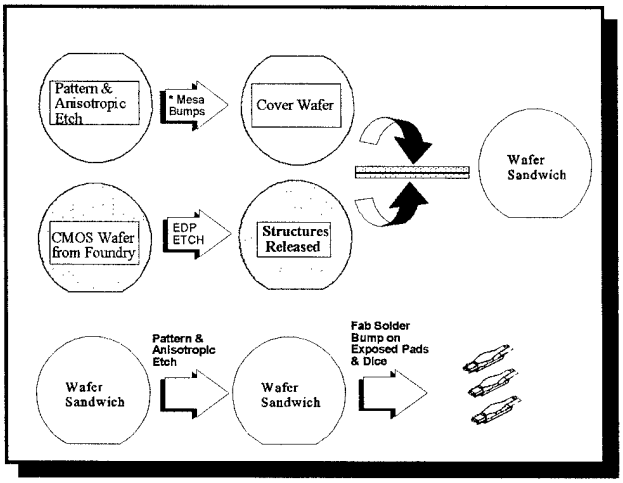


**Figure 4.4** Generalized Post CMOS Process

As with the MEMS rules addition to the MOSIS process, specialized rule violations are needed. However, different than the MEMS rules, our need is to preserve intermediate layers rather than using nitride as the principal MEMS material. Because documentation is limited, effects uncertain, and repeatablity unqualified, many alternative trial designs are warranted. The more conservative approaches are reported.

Although initial designs were with AutoCAD, better and quicker results were obtained with the Tanner Pro Software L-EDIT. Color screen dumps which are annotated help to present these results. Figure 4.5 provides a common legend for the plots.

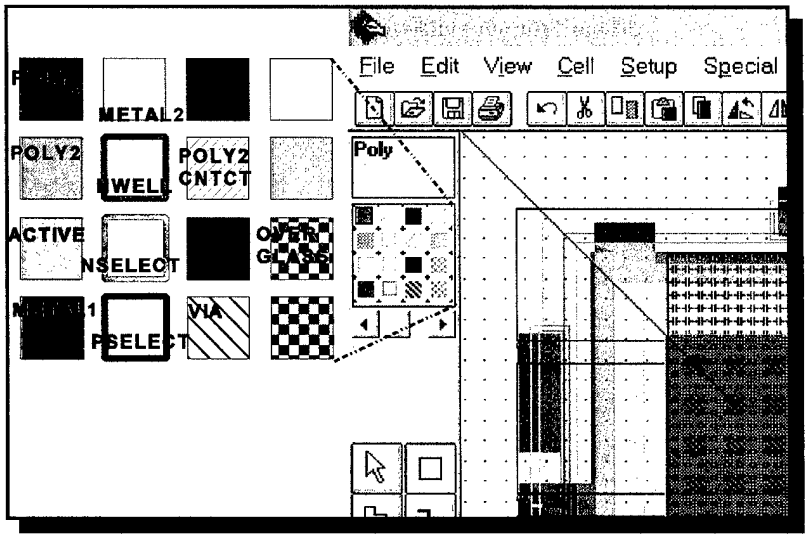


**Figure 4.5** Legend for Layout Plots

### 4.2.1 Piezoresistive sensor

Guckel ('92) performed detail study of the residual stress in polysilicon layers and the effect of the stress on diaphragms. His application was in piezoresistor sensors with polysilicon diaphragms over sacrificial oxide. Thicker layers than available within the target CMOS process were used but the diaphragm equations provided are useful. His evaluation of stress in polysilicon as a function of process temperature and time is also useful. The values and results for polysilicon layers in a 0.8 μm CMOS process (Biebl,'95) were similar.

Equation 1, derived from Guckel, provides the relationship between the peak deflection, $\omega_{max}$, at the center of a square diaphragm versus pressure and residual stress.

$$\omega_{max} = \frac{0.0152 \cdot q \cdot a^4 \cdot \frac{(1-\nu^2)}{E \cdot h^3}}{\left[1 + \frac{9 \cdot a^2 \cdot (1+\nu) \cdot \varepsilon_{res} \pi^2 \cdot h^2}{4}\right]^{-1}} \quad (1)$$

where $q$ is pressure, $a$ is the length of a side, **h** is diaphragm thickness, $\nu$ and $E$ are the normal material constants, and $\epsilon_{res}$ is the residual stress.

Equation 2 determines the critical relation between compressive residual stress and buckling of the diaphragm.

$$a_\infty = h \cdot \sqrt{\frac{-4\pi^2}{9 \cdot (1+\nu) \cdot \varepsilon_{res}}} \quad (2)$$

where the variables are the same as equation 1 and $a_\infty$ is the critical length. Using these relationships, design parameters for the diaphragm were evaluated. The CMOS design rules provided the layer thicknesses and separation between layers with tolerances. Thus, the design choices were limited to selecting which layers are used for structural material and which are sacrificial, subject to their interaction with fixed and selectable process steps. Remaining selectable design parameters are the length and geometry in all but thickness.

By choosing conservative estimates for residual stress values and keeping length less than approximately 85% of the calculated critical value $a_\infty$, acceptable designs were obtained. The results yielded limits for diaphragms of 100 μm square when constructed with the N-well diffusion material. For 0.4 μm polysilicon (transistor gate material), conservative diaphragm length without buckling risk is 20 μm.

The N-well diffusion will be exposed by the anisotropic etch when chip sculpting is performed. This construction provides a simple port to the unknown pressure. The diaphragm only is exposed to dirty air media.

Design provisions include a means to bias the N-well during IC sculpting. The biased N-well diaphragm will electrochemically stop the etch when it forms a pn junction with the etch liquid upon exposure. Although the pn junction bias theoretically provides excellent thickness control in anisotropic etch, variations in current densities and voltage introduce variation in the final result (Ma,'94, Riou,'92).

Equation 3 determines the responsivity of the peak strain at the center edge of the diaphragm. This is where polysilicon or diffused piezoresistors should be placed. The responsivity of the diaphragm strain (determined for N-well diaphragm $a$ = 100 μm ) is $1.75 \cdot 10^{-5}$ /psi. Analysis of the sensitivity of the response in strain for variation in the diaphragm length, equation 4, is determined by the partial derivitive,

with respect to ***a***, of equation 3

$$\epsilon_{x_{max}} = \frac{0.308 \cdot q \cdot a^2 \cdot \frac{(1-\nu^2)}{E \cdot h^2} \cdot}{[1 + \frac{9 \cdot a^2 \cdot (1+\nu) \cdot \varepsilon_{res}}{4} \pi^2 \cdot h^2]^{-1}} \quad (3)$$

$$\frac{\partial \epsilon_{x_{max}}}{\partial a} = \frac{0.616 \cdot q \cdot a \cdot \frac{(1-\nu^2)}{E \cdot h^2} \cdot}{[1 + \frac{9 \cdot a^2 \cdot (1+\nu) \cdot \varepsilon_{res}}{4} \pi^2 \cdot h^2]^{-1}} \quad (4)$$

Variables fixed by fabrication steps are length ***a*** and thickness ***h***. The design rule tolerance applies for ***h***. Length ***a*** is critically dependent upon the wafer thickness by the geometry of the <111> etch planes with respect to the <100> wafer. As it turns out $\epsilon_{x\_max}$ sensitivity is strongest to variations in ***a***. With typical variations of 50 μm in wafer thickness, then multiplied a factor of approximately $\sqrt{2}$ due to geometrical relationships, length ***a*** contains the worst case variation as well. An error of 1 μm in the diaphragm length is equivalent to miscalibration by 1 psi. Masks openings which define the diaphragm need to be adjustable after measurement of individual wafers to achieve the necessary control of sensor performance. Placing the sides of the released diaphragm in precise alignment of the piezoresistors is also critical. Sensitivity to remaining process variable errors or tolerances is easily done by similar mathematics.

Figure 4.6 shows an L-Edit layout of the resultant sensor cell. The cross section view has been annotated to show the anisotropic etch exposure of the N-well from substrate side. Final release and definition of the diaphragm occurrs in surface micromachining before joining the cover wafer and CMOS wafer as was shown previously in Figure 4.4. Ethylene Diamine Pyrocatechol can be used to remove whatever metal 1 and poly 2 layers remain after the CMOS process etches the pad overglass cuts without underlying metal 2. Although similar in size to normal CMOS I/O pad masks, the design rule for metal 2 overlap of the overglass is violated and metal 1 is exposed to the overglass removal etchant and may be attacked by it. Process experiments were planned and a test chip (see subsection 4.3) developed for this purpose.

Overpressure stops can be built into the cover wafer as bumps or mesas left protruding above a surface etched a little more than 1 μm deep. Exact value depends upon the thickness of layers in the CMOS wafer. Alternatively, the overstop may possibly be fabricated in the CMOS structure. Partial windows in via and overglass layers will leave oxide plate supported by oxide bridges after EDP surface etching. The separation from the diaphragm (i.e., the limit of $\omega_{max}$ is set by the poly 2 layer thickness, 0.4 μm which is the appropriate value).

### *4.2.2 Capacitive sensor*

Figure 4.7 shows the layout for a capacitively sensed pressure sensor. It is similar in size to the piezoresistor based sensor described previously. Equations 1 and 2 above apply in the design of the diaphragm and air gap (vacuum) capacitor.

Incorporating equation 1 into the equation for capacitance allows investigation of $\omega_{max}$ responsivity to the process tolerances and error factors.

This is easily done by expanding partial derivitives of the equation in Taylor series about each variable. Equations 5 through 8 present the sensitivity (responsivity) of $\omega_{max}$ to pressure ***q***, length ***a***, thickness ***h***, and residual stres $\epsilon_{res}$

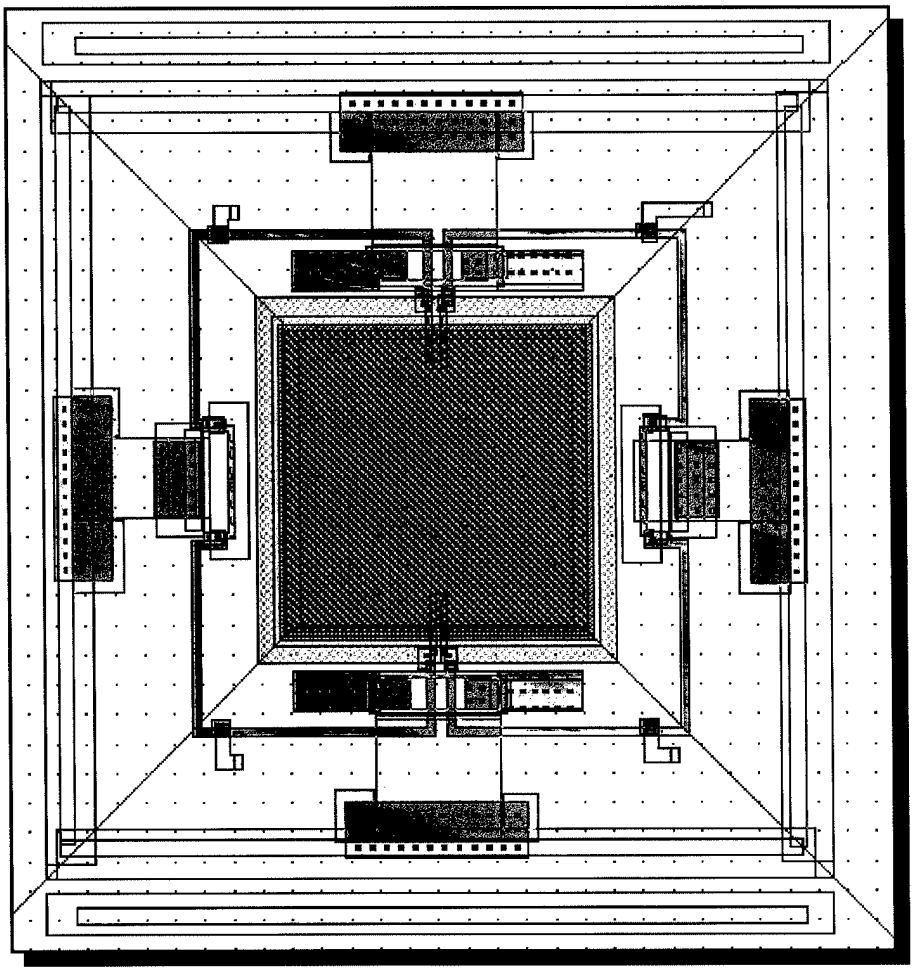

**Figure 4.6(a)** L-Edit Layout of Piezoresistive Sensor

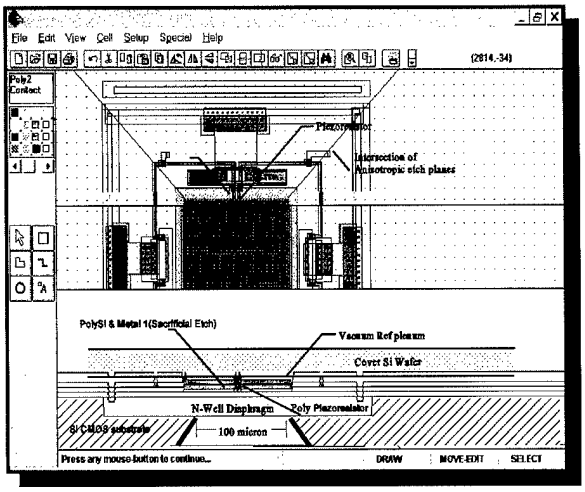


**Figure 4.6(b)** Cross Section of Sensor

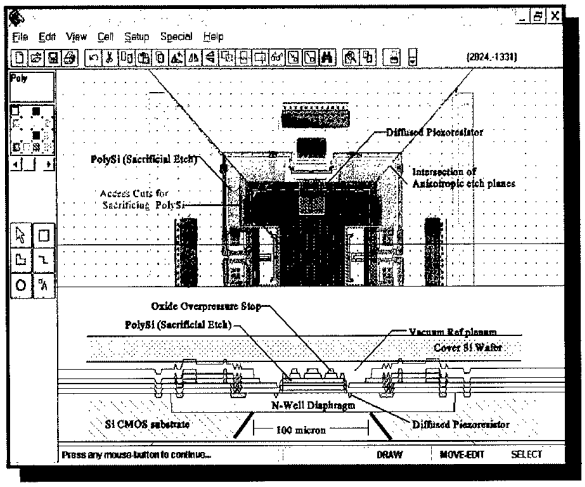


**Figure 4.6(c)** Sensor w/ OverpressStop

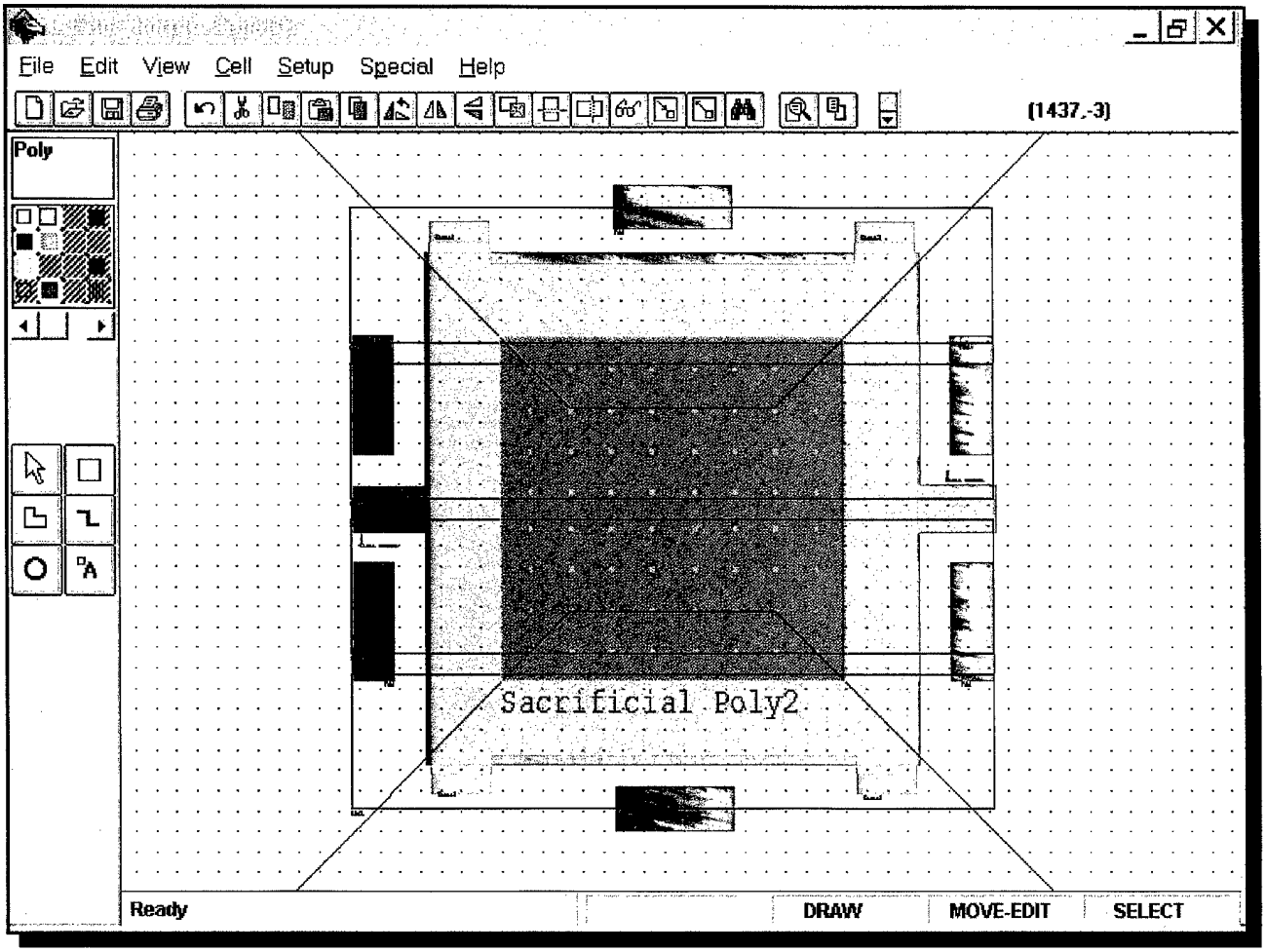


**Figure 4.7(a)** Capacitive Pressure Sensor Based on $XeF_2$ Surface Micromaching of CMOS

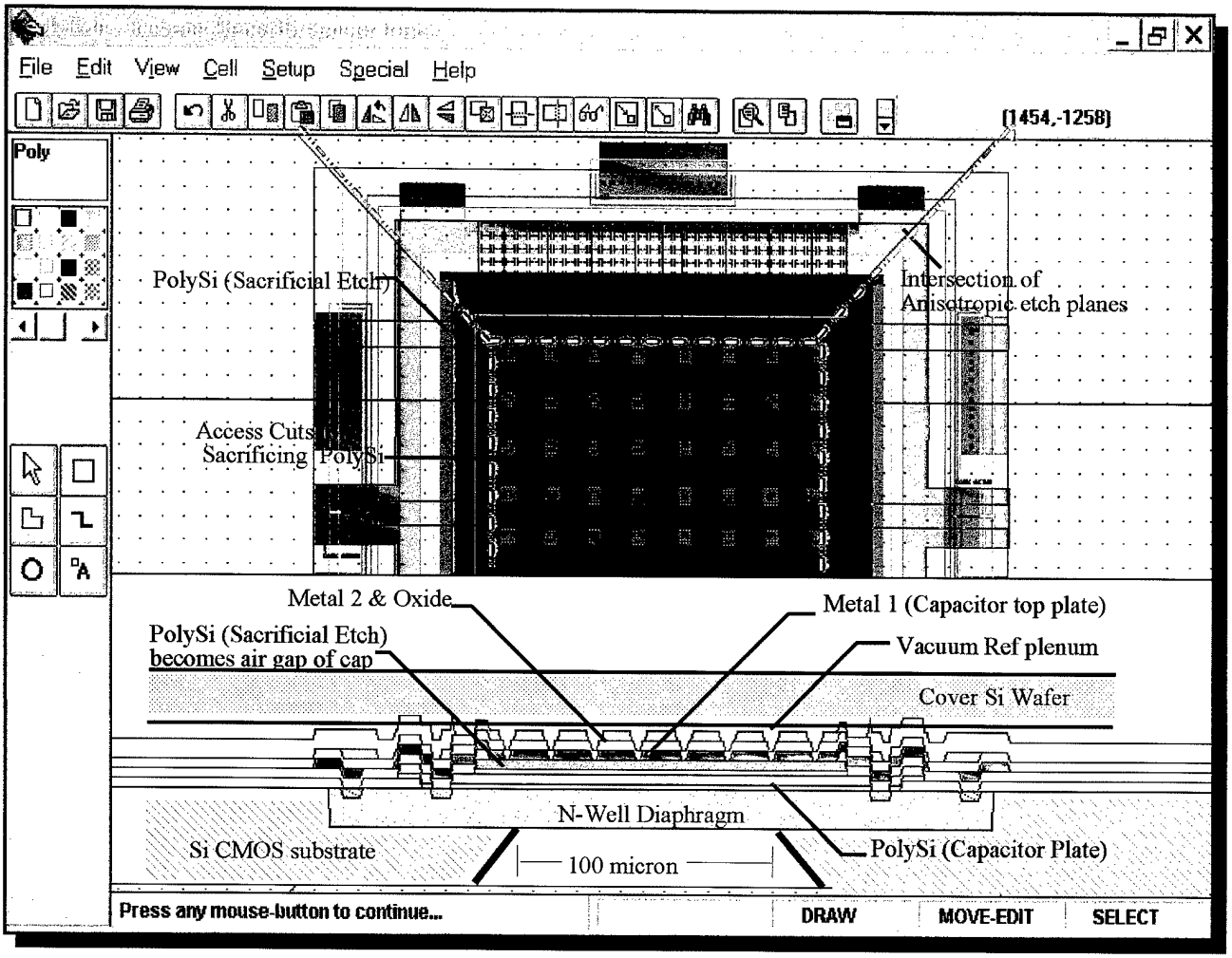


**Figure 4.7(b)** Cross Section of Capacitive Sensor Assembly

respectively. Sensitivity to pressure change, $r_q$ (%C/δ psi), is 0.28% / psi (0.00126 pf/ psi) at 47 psi (324 kPa) operating pressure. Sensitivity to error in the diaphragm length, $r_d$, is 4.6 %C / μm. Residual stress change of 0.001 will produce a negative shift, $r_\epsilon$ , of 1.32% in calibration whereas 0.1 μm variation in the N-well thickness is -5.33% change, $r_h$, in capacitance at this pressure condition.

$$r_q = 1.52\cdot10^{-2}\cdot\frac{\varepsilon_0}{d^2}\cdot\frac{(1-\nu 2)}{(E\cdot h^3)}\cdot a^6 + 3.47\cdot10^{-3}\cdot\frac{\varepsilon_0}{d^2}\cdot\frac{(-1+\nu^2)}{h^5}\cdot\varepsilon_{res}\cdot\frac{(1+\nu)}{E}\cdot a^8 \quad \textbf{(5)}$$

$$r_a = 2\cdot\frac{\varepsilon_0}{d}\cdot a + 9.12\cdot10^{-2}\cdot\frac{\varepsilon_0}{d^2}\cdot q\cdot\frac{(1-\nu^2)}{(E\cdot h^3)}\cdot a^5 + 2.77\cdot10^{-2}\cdot\frac{\varepsilon_0}{d^2}\cdot q\cdot\frac{(-1+\cdot\nu^2)}{h^5}\cdot\varepsilon_{res}\cdot\frac{(1+\nu)}{E}\cdot a^7 \quad \textbf{(6)}$$

$$r_h = 4.56\cdot10^{-2}\cdot\frac{\varepsilon_0}{d^2}\cdot q\cdot\frac{(1-\nu^{20}}{(E\cdot h^4)}\cdot a^6 + 1.73\cdot10^{-2}\cdot\frac{\varepsilon_0}{d^2}\cdot q\cdot\frac{(-1+\nu^2)}{h^6}\cdot\varepsilon_{res}\cdot\frac{(1+\nu)}{E}\cdot a^8 \quad \textbf{(7)}$$

$$r_\varepsilon = 3.47\cdot10^{-3}\cdot\frac{\varepsilon_0}{d^2}\cdot q\cdot\frac{(-1+\nu^2)}{h^5}\cdot\frac{(1+\nu)}{E}\cdot a^8 \quad \textbf{(8)}$$

where ***a, h, E, ν,*** $\epsilon_{res,}$ and ***q*** are as previously defined. New variables $\epsilon_0$ and ***d*** are permitivity of vacuum and capacitor plate separation, respectively.

The above relations underscore the importance of managing the design and fabrication factors as well as possible to obtain suitable capacitance sensing performance and conversion to an accurate pressure output. Other relations (e.g, temperature coefficient of Young's modulus, ***E***, and zero pressure plate separation, ***d***, a function of poly 2 thickness tolerance and contact etch selectivity) need examination as well. $\omega_{max}$ shows great sensitivity to any variation in diaphragm length ***a*** and thickness ***h***. If typical variations of 50 μm in wafer thickness are expected, then 70 μm, or 70%, change results without active manufacturing adjustment. Although some researchers have used buried layers to create accurate masking of known thickness layers, this technique is not likely an option. Laser measurement scanners typically measure with spot size of 0.1 mm so it is feasible to get accurate measurement at every sensor site on the wafer. Mask openings, which define the diaphragm, need to be adjustable after measuring

wafers to achieve the necessary control of sensor performance

In addition, the variations in N-well thickness and bias effects in the electro-chemical etch stop produce significant variations in the parameter ***h***. The circuit connection to the N-well to provide the etch stop bias voltage needs to be well designed and implemented to reduce this error. Ma ('95) has designed a capacitive electro-chemical etch stop means which may be feasible to implement. These factors, along with inherent non-linearity of response from capacitor sensing of this type, require high sensitivity conversion from the analog processing electronics. A capacitor model (equation 10) derived from analytic solutions (equation 9) to the shape of loaded square membranes (Dietre,'95) show the non-linearity of capacitor output with pressure. Figure 4.8 is an example.

In this design, it is vital to employ processes which do not damage metal 1, the capacitor top plate or the bottom poly/substrate capacitor plate. The main process issue needing resolution is the effect of various mask patterns for via and overglass layers in the CMOS process. This hinges on two factors. First is the selectivity of the oxide etchants used in making poly 2 contact. Over-etch or poor selectivity will vary the capacitor plate separation, $d_0$. Also important is selectivity of via and overglass etchants (known to attack poly and silicon layers). This is important because, although poly 2 is a sacrificial layer, the design intends that it remain relatively intact to protect lower layers. Also the very gentle $XeF_2$ gas phase can be used for the final etching to form the capacitor gap. Recent techniques with CMOS circuits using $XeF_2$ vapor phase etching of polysilicon have been successful at UCLA (Chang,'95, Chu,'96, Kruglick,'95).

Test chips fabricated in the MOSIS and/or Foresight process can provide insight into the feasibility of this type of capacitor sensor. A test chip has been designed. It contains several similar capacitor structures and test stackups. The variations in the stackup and geometry of defining masks for vias, metal 1 and metal 2 patterns, and overglass openings provide some means to initially evaluate these effects.

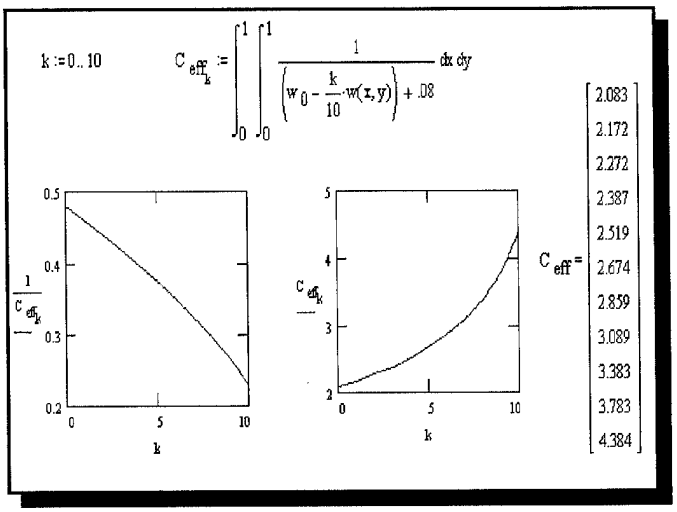


**Figure 4.8** Capacitance of Pressure Loaded Square Diaphragm vs 1/10 Full Scale Pressure Increments

$$\omega = \omega_0 \cdot (1 + \omega_1 \cdot \frac{x^2+y^2}{a^2} + \omega_2 \cdot \frac{x^2 \cdot y^2}{a^4}) \cdot \cos(\frac{\pi \cdot x}{2 \cdot a}) \cdot \cos(\frac{\pi \cdot y}{2 \cdot a}) \quad (9)$$

$$C_{eff_k} = \int_0^{\wedge} \int_0^{\wedge} \frac{1}{\omega_0 - \frac{k}{10} \cdot \omega(x,y) + .08} dxdy \quad (10)$$

### 4.2.3 Capacitive sensor/actuator

Sensor/ actuators are frequently used in re-balance closed loops in high precision sensors and measurement instruments. The advantage is that closed loop processing keeps operaton at a fixed operating bias point. Small deviations from the fixed point are easily detected but are not necessarily required to be accurately calibrated. Provided there is an accurate measure of the rebalancing signal (force), the effect of the errors discussed above is significantly reduced (UCLA,Feb'96, Weijie,'92). Given the self-test requirements for this sensor, our studies investigated the potential for force rebalancing a capacitor diaphragm of the type previously discussed.

However, the direct Coulomb acctracting force resulting from applied voltage (equation 11) between the capacitor plates of the design above is the opposite of a rebalancing force. Its magnitude is small compared to pressure forces (as given in equation 12). Therefore, the only

$$F_c = -0.5 \cdot \varepsilon_0 \cdot V^2 \cdot \frac{A}{z^2} \qquad \textbf{(11)}$$

$$F_p = A \cdot p \qquad \textbf{(12)}$$

viable consideration for an electrostatic rebalancing actuator is to provide a separate forcing structure attached to the diaphragm. The structure must be capable of generating larger forces than the maximum pressure force. So for an electrostatic actuator, it must provide capacitor plate area very much larger than the area of the sensitive diaphragm. An example is a surface normal actuator (Gabriel,'92).

The CMOS design rule parameters provide two alternatives which are potentially materials for shorter length sensitive diaphragms and correspondingly thinner to maintain sensitivity. Either 0.4 μm poly layers or source/drain diffusions in the either of the substrates can be considered.

The CMOS gate/conductor polysilicon layers were tried for diaphragms but this was found to be much too complicated—even on a conceptual basis. However, a modification to the design above can produce a diaphragm from p or n diffusions. Active contacts with metal 1 can attach an oxide structure to apply rebalancing forces. This concept is as notionally presented in Figure 4.9 on the following page.

We have also considered adding an appropriately selected fluid of high dielectric constant between the plates to increase the force with less voltage. To achieve suitable results, a dielectric constant greater than approximately 20 is required. With a large dielectric constant multiplication, cascaded voltage doubler circuits, and large area overhung plate, it is conceptually possible to provide closed loop force rebalance across the complete tire pressure spectrum. But there are significant issues related to this active sensor/ actuator.

### 4.3 Electronic Circuit Design and Simulation

The test chip design requirements were:

(1) Integrate structures consistent with the physical constraints imposed by Sure✓™ valve stem design;
(2) use low-cost multi-user CMOS IC fabrication;
(3) buffer the MEMS sensor from the external equipment loading and drive interfaces;
(4) provide for alternate sensor measurement circuit techniques to be evaluated with the test chip;

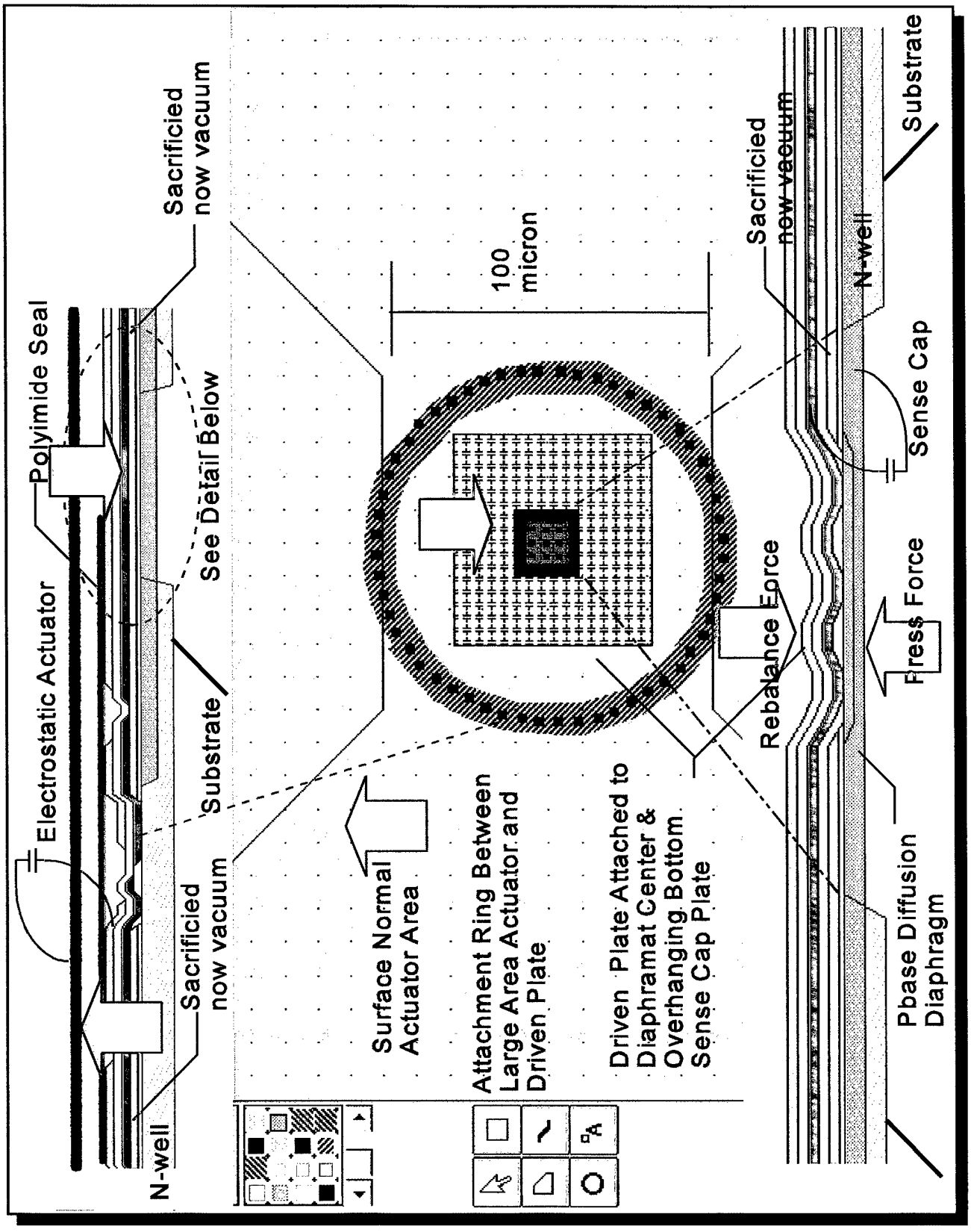


**Figure 4.9** Conceptual Sensor with Force Rebalance Actuator

(5) Integrate representative analog circuitry functions available in standard CMOS processing and evaluate.

### *4.3.1 Analog Circuit Design*

The analysis of sensors provided above defines analog constraints for circuits discussed below.

#### *4.3.1.1 Capacitive Sensor Measurement*

We found two measurement methods in the literature for measuring the capacitance change of capacitive sensors: integrated capacitance bridge (UCLA MEMS Feb '96) and charge redistribution sensing (Kung,'92).

Both of these measurement methods require two identical capacitors. Pressure acts on one capacitor and produces a difference be-tween the capacitance values. The output of the measurement circuits is proportional to the difference capacitance divided by the fixed capacitance. We refer to the pressure dependent capacitor as the sense capacitor. The pressure independent capacitor is the reference capacitor. By making the capacitors with the same structure and geometry, pressure independent variations cancel.

##### *4.3.1.1.1 Integrated Bridge Measurement*

The integrated bridge measurement method applies a balanced AC drive to the series connection of the two capacitors. The voltage at the center connection depends on the capacitance imbalance and provides the output measurement.

A balanced drive in CMOS is obtained by operating N-Channel and P-Channel MOSFETS as switches in a transmission gate circuit. The transmission gate turns on or off both transistors from a single logic level enable signal. For each drive node, two transmission gates are connected to two power supplies voltages. By periodically enabling the transmission gates in pairs, the balanced AC drive required is produced.

We cannot directly measure the output voltage of the bridge due to the loading effect of stray capacitance. The sensor and reference capacitors are only a couple of pico-Farads and would be significantly loaded by just the IC pin capacitance (typically 5-10 pF) not to mention stray capacitance due to external wiring. Standard linear CMOS functions include operational amplifiers (op amps) which can be used to isolate the sense node voltage from the pin and external load capacitance.

Figure 4.10 presents a block diagram for the integrated bridge capacitance measurement approach applied to an integrated device (the test chip). Transmission gates T1-T4 perform switching functions, driving the series connected sense and reference capacitors to provide the voltage signal at the input of analog buffer U1 representing a non-inverting voltage follower op amp circuit. The $V_{REF}$ voltage determines both the gain and the DC offset of the circuit. Setting $V_{REF}$ equal to $V_{CC}$ provides the maximum output signal and a common mode input voltage to the op amp at half its supply voltage where its For small changes in capacitance with pressure, $\delta C$ performance should be optimal. For small changes in capacitance with pressure, $\delta C$ small compared to $C_{ref}$, the AC signal amplitude (pk-pk) at the input of the analog buffer U1 is:

$$V_{\cdot\bullet} = \frac{V_{\ell^{\circ}\mu} \cdot \delta C}{2 \cdot C_{\ell^{\circ}\mu}} \qquad \textbf{(13)}$$

Off the test chip, an over sampling analog to digital converter provides the input to a digital

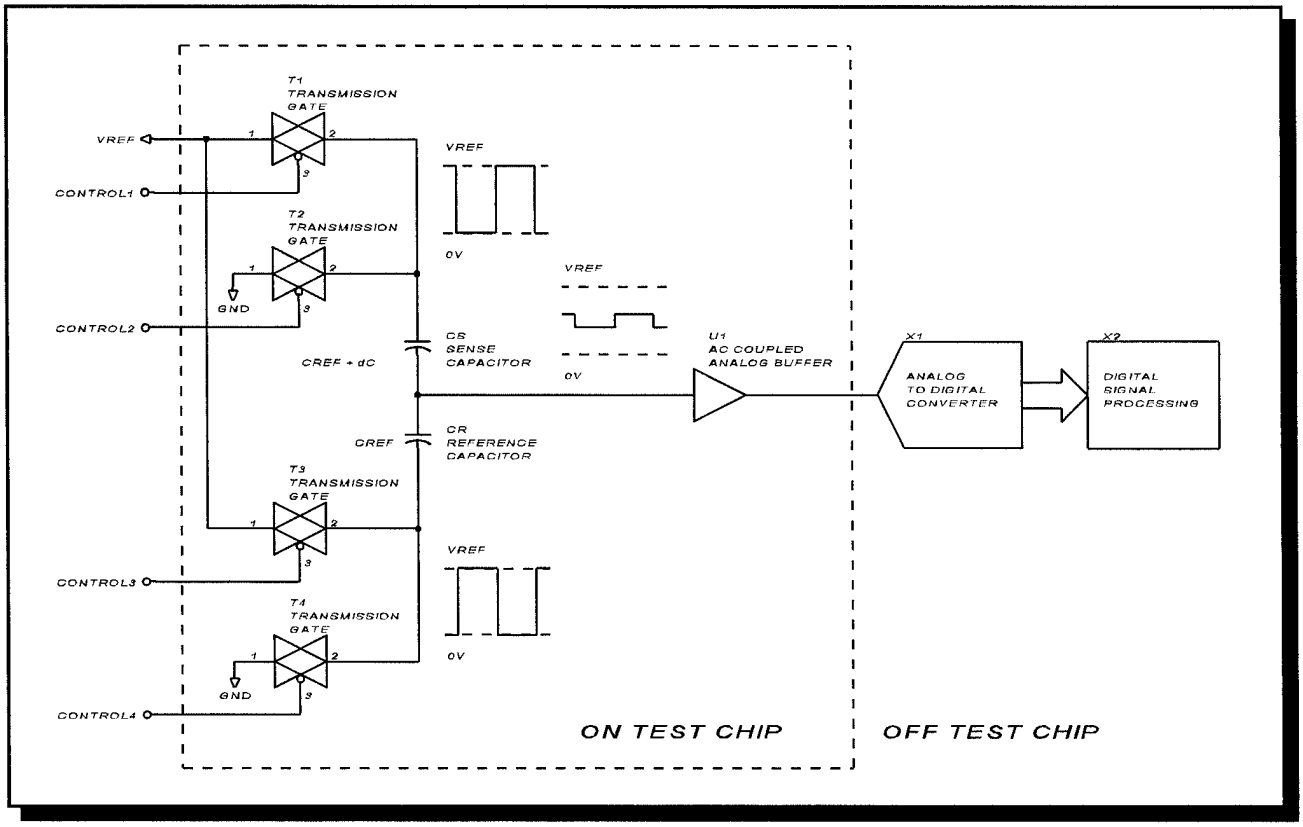


**Figure 4.10** Integrated Bridge Capacitance Measurement

signal processing block which demodulates the output signal. Alternately, the output signal can be demodulated prior to digitizing which may improve SNR, simplify the required digital processing, with the addition of more analog circuitry.

The following on chip circuit effects are significant to the operation of this bridge circuit:

(1) Signal amplitude versus input and output range of the op amp.

The op amp must provide a larger input and output signal range than that produced at the sense node for proper operation.

(2) Op amp offset voltage non-linear dependence on input voltage.

Non-linearities in offset voltage produce gain variations and errors that are not canceled by demodulation.

(3) Op amp bandwidth versus control frequency.

The transmission gate circuits must be controlled at a frequency which does not exceed the bandwidth of the op amp buffer.

(4) Stray Capacitance on the sensor output node.

Stray capacitance will reduce the signal gain and contribute to DC offset in the sensor output signal.

(5) Op amp input bias voltage.

The DC op amp voltage is not guaranteed since it is capacitively coupled and the typical CMOS op amp input terminals are MOSFET gates. The bias voltage is easiest established in a standard CMOS process (without a high value sheet resistance available) by adding a DC restore function with one or more transmission gates connected

to the sensor output node. Adding these gates may produce leakage current which can limit the minimum AC drive control frequency due to drift of the sensor output node.

#### 4.3.1.1.2 Charge Redistribution Measurement

The charge redistribution measurement method is similar to the integrated bridge method except that a difference charge provides the output signal rather than a difference voltage. The common node of the series connected sense and reference capacitors is connected to the summing junction (inverting input) of an amplifier. Additionally, a feedback capacitor is added between the amplifier output and the summing junction. The output of the amplifier drives the feedback capacitor in order to inject enough charge into the summing junction to maintain the inverting input at the voltage of the non-inverting input. One can think of this circuit as equivalent to the integrated bridge circuit with the addition of an inverting buffer with gain set by the ratio of the feedback capacitor to the capacitance bridge.

What makes this a charge redistribution circuit is the replacement of the op amp with a comparator driving a successive approximation register driving a digital to analog converter which drives to the feedback capacitor. As the successive approximation register is updated, the DAC output changes and the charge of the capacitors is redistributed. If a positive charge remains relative to the non-inverting input voltage, the comparator slews low indicating that the value is too high. If the charge is negative, the compara-

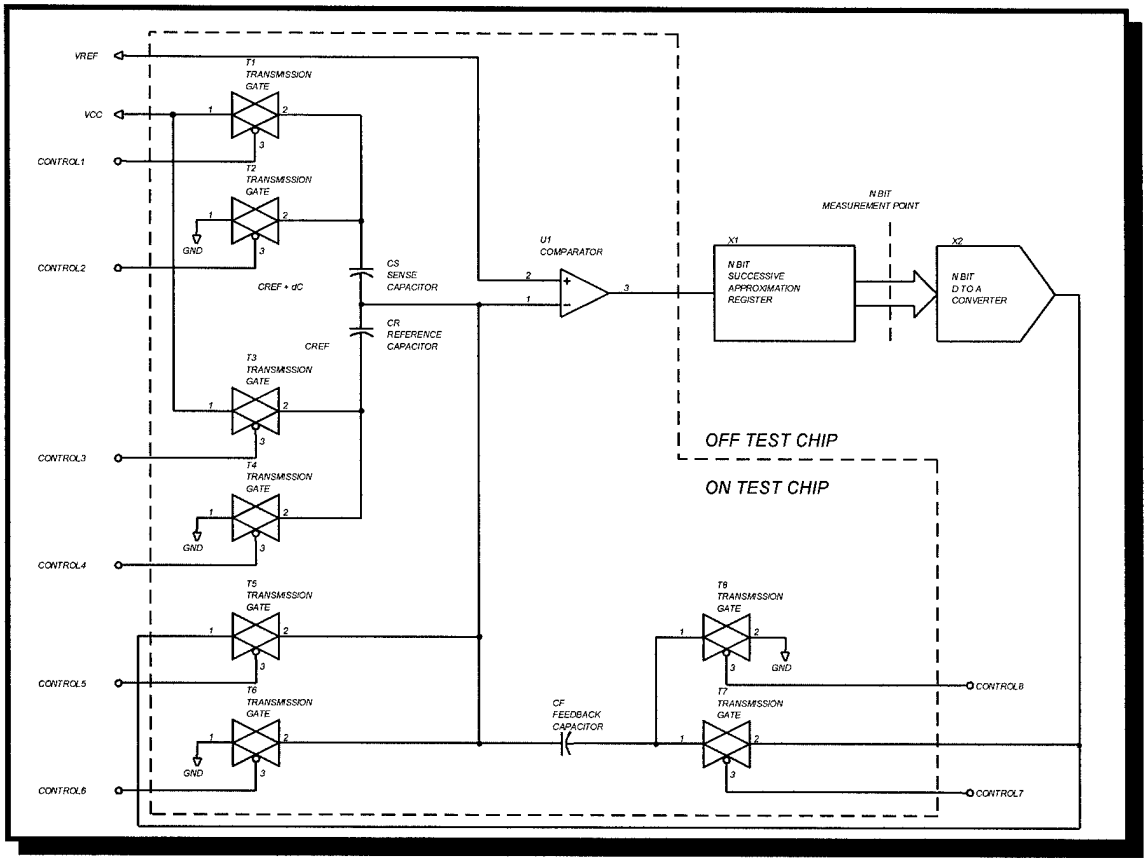


**Figure 4.11** Charge Redistribution Capacitance Measurement

tor slews high, indicating that the register value is too low. An N-bit measurement is made directly, by testing each of the bits, one at a time, from MSB to LSB and continuously updating the successive approximation register with the result of the test.

As with the integrated bridge circuit, the charge redistribution circuit is made up of easily integrated CMOS circuits: transmission gates and a comparator instead of an op amp. Since an op amp can be operated as a comparator, these circuits can be integrated with identical macrocells.

Figure 4.11 presents a block diagram for the charge redistribution capacitance measurement approach.

The operation of the circuit is as follows:

(1) Set $V_{REF}$ to ½ supply voltage and load equivalent value into successive approximation register X1 to produce $V_{REF}$ output at X2.
(2) Enable transmission gates T1, T4, T5, and T7 discharging the feedback capacitance and DC restoring the common sense node at $V_{REF}$.
(3) Disable transmission gate T5 which puts CF in the feedback loop.
(4) Disable transmission gates T1 and T4 while enabling transmission gates T2 and T3. This charges the summing node of the op amp with the difference charge.
(5) Wait for settling time of U1 then sample output for high or low level. If high, set successive approximation register for $3/2 \cdot V_{REF}$. If low, set successive approximation register for $½ \cdot V_{REF}$.
(6) Continue process to determine each bit of the successive approximation register.

The resulting digitized difference measurement voltage is:

$$V_0 = \frac{V_{REF} \cdot \delta C}{C_F} \qquad \textbf{(14)}$$

One cancels offset in the reading by setting the DAK back to $V_{REF}$, enabling T1 and T4 while disabling T2 and T3 and repeating the measurement sequence of steps 5 and 6. Alternately, the DC restore can be made with T2 and T3 on and interchanging T1 and T2 states along with T3 and T4 states. This produces an opposite initial bias on the sensor capacitance allowing for the potential measurement and calibration of sensor deflection due to Coulomb forces with opposite voltages applied.

The comparator output can also be connected directly to the feedback point to providing an analog signal with the same gain. This configuration requires analog to digital conversion after the amplifier. Restoring the voltage in alternate T1 - T4 states produces the largest signal swing at one half the frequency.

The charge redistribution circuit has the same significant effects from on-chip sources as the bridge circuit.

### *4.3.2 Test Chip Analog Circuit Design*

Because of the similarities in the circuitry required to operate the capacitive sensor, we developed a common circuit capable of performing both measurement functions. This circuit appears in Figure 4.12.

The test chip schematic combines transmission gates, capacitive sensors, and op amp circuitry allowing both capacitive measurement ap-

proaches to be implemented with the appropriate external signal connections to the test chip. Note that the sensor capacitor consists of a fixed and variable (pressure dependent) capacitance, $C_{SENSEF}$ and $C_{SENSEV}$. Also note the addition of stray capacitances estimated from the capacitor geometry and interconnect.

Op amp, XAMP1, is configured as a unity gain analog buffer and provides the analog voltage output, $V_{OUT}$ for the integrated bridge capacitance measurement. The second op amp, XAMP2, operates as a comparator providing a digital voltage output, $D_{out}$ for the charge redistribution capacitance measurement.

Both op amps require current setting bias voltages supplied by the bias splitter circuit XSPLIT. The input to this circuit is an N-Channel MOSFET gate bias referred to ground and a cascode N-Channel gate voltage. Its output voltages are N and P channel biases to the respective supplies along with cascode N and P channel gate bias voltages. The op amps require these voltages to set their internal bias currents.

XBIAS generates the input n-channel MOSFET gate to source bias for XSPLIT. In order to assure that XBIAS always starts, startup circuit XSTART monitors a p-channel gate to source voltage, and provides a start current if the monitored voltage is below a threshold value.

The startup circuit was included after analysis and simulation of the macrocell indicated a potential startup problem due to an unstable equilibrium point of the circuit with zero gate to source voltage.

A set of 2 micron n-well and p-well CMOS macrocells available from the Tanner L-Edit layout and simulation tool suite provided the basis for each of the macrocell designs. This is considered to be the lowest risk approach to the electronic design to use available macrocells and only modify where analysis indicated modification was necessary for proper operation.

The results of the analysis of each of the macrocells is presented in the following sub-sections followed by a discussion of whole chip simulation results.

### *4.3.2.1 Macrocell Circuit Analysis*

Analysis and simulation of macrocell models, in independent circuit operating, provided design parameter data. L-Edit and Spice extraction captured the model geometries from the macrocell layouts.

#### *4.3.2.1.1 I/O Pad Macrocell*

Figure 4.13 provides a schematic for the Input/ Output pad macrocell. Each I/O pad contains large geometry NMOS and PMOS transistor devices biased off, providing diode clamping of the input to the supply and ground. These devices provide limited protection of smaller geometry integrated devices in the chip to over voltage and over current pin conditions but do assure that charge will not build up on unconnected pins. The I/O pad macrocell is based on geometries associated with an existing Tanner library macrocell (Tanner Pro Software Library,'96). We also used two related pin macrocells shown schematically as ppad.sch and bpad.sch. The ppad represents power pin connections for $V_{CC}$ and GND which do not include clamp transistors and have a larger capacitance due to large geometry metal lines which connect to the pad. The bpad consists of an iopad without the protect resistors but with the same pad capacitance.

Table 4.2 tabulates the results of TSPICE simulations for the iopad macrocell for performance

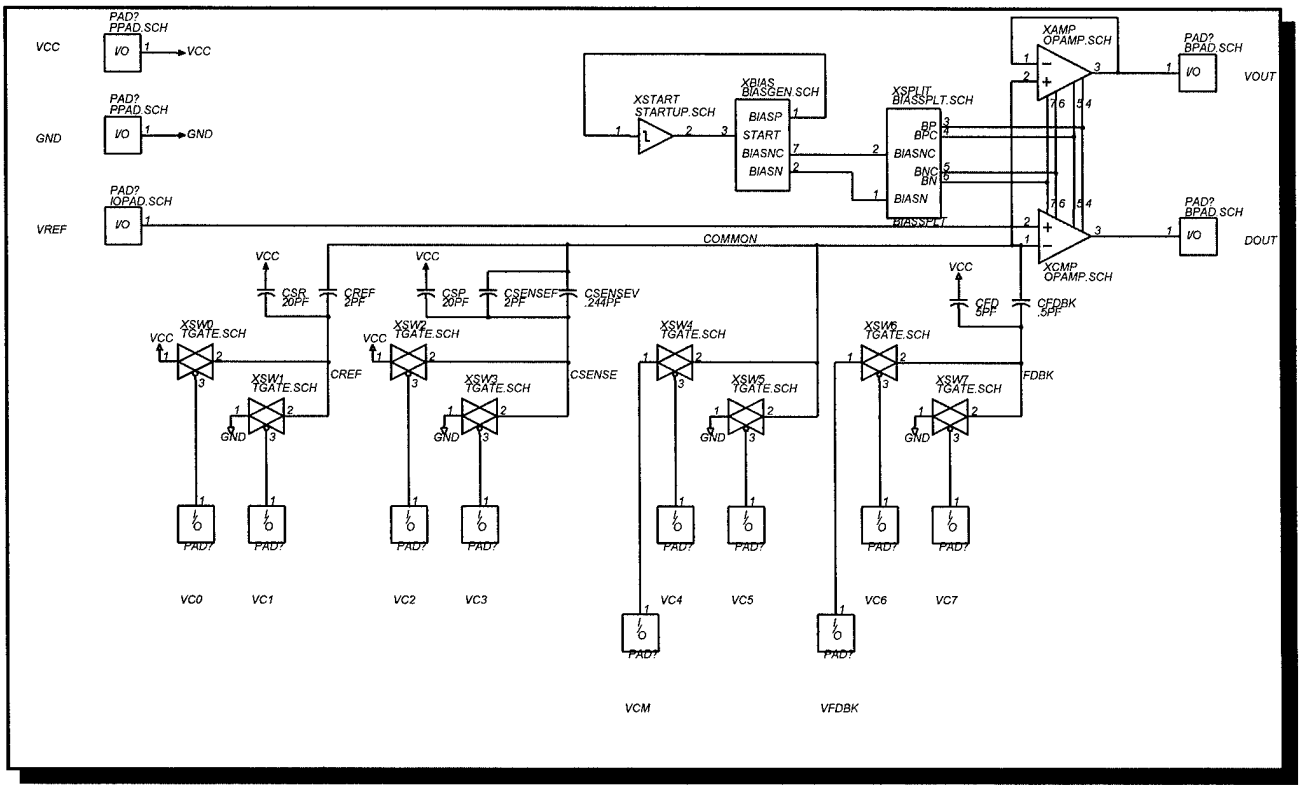


**Figure 4.12** Top Level Test Chip Schematic

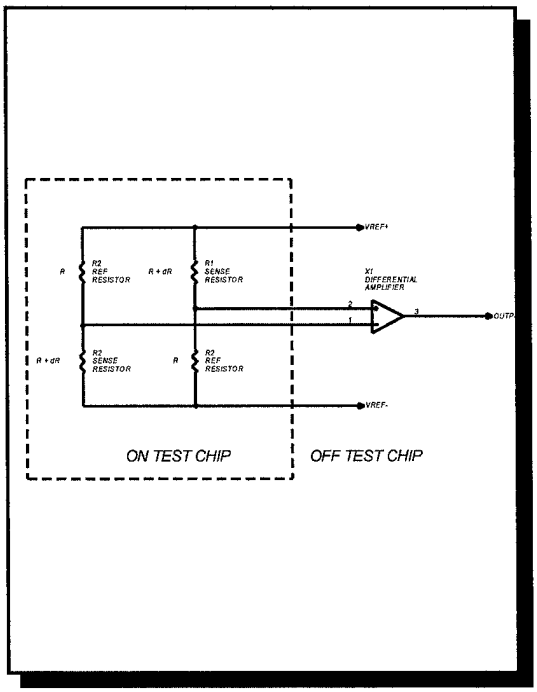


**Figure 4.13** IO Pad Macrocell Schematic

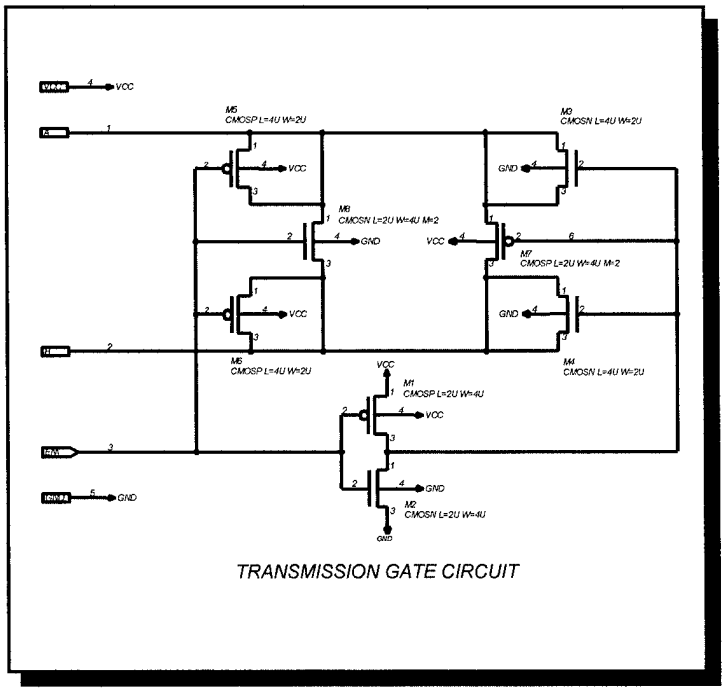


**Figure 4.14** Transmission Gate Macrocell Schematic

| IO Pad Macrocell Simulation Results (VCC = 5V; 27°C) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Units** |
| $I_{L1}$ | Leakage Current | | <<10 | | fA |
| $I_{L2}$ | Leakage Current @ -40°C | | <<10 | | fA |
| $I_{L3}$ | Leakage Current @ 70°C | | 11 | | fA |
| $C_S$ | Stray Capacitance | | .31 | | pF |
| $V_{INH}$ | Clamp Voltage High (1 uA) | | 6.3 | | V |
| $V_{INL}$ | Clamp Voltage Low (1 uA) | | -1 | | V |

**Table 4.2** I/O Pad Macrocell Simulation Data

parameters. This data shows extremely low leakage currents observed due to the clamp transistors which are nominally biased off. Stray capacitance due to the transistors is approximately 20 fF. The clamp voltages are well within the process breakdown limits which are greater than 10V.

All of these parameters are well within operating requirements and there are no significant issues related to the macrocell operation or usability in the fully integrated sensor.

#### *4.3.2.1.2 Transmission Gate Macrocell*

Figure 4.14 provides a schematic for the transmission gate macrocell. The transmission gate function is provided by PMOS transistor M7 and NMOS transistor M8. Transistors M1 and M2 provide a CMOS inverter to allow a single active low enable circuit to turn on both transmission gate transistors. Transistors M3 - M6 provide charge injection compensation and diode clamp the transmission gate nodes to $V_{CC}$ and GND. The I/O transmission gate macrocell is an existing Tanner library macrocell.

Table 4.3 tabulates the results of TSPICE simulations for the transmission gate macrocell for performance parameters. This device's switching times limit the maximum frequency of the capacitance measurement systems. The longest time of 20+ ns, corresponds to an operating frequency of 25 MHZ which is well in excess of the expected op amp capability. The load is based on the estimated sense or reference capacitor values.

The switching times are due to the on resistances which were calculated based on an exponential fit to the switching waveforms. With no appreciable static channel current, these values are only significant for their effect on the switching characteristics. Should faster switching times be required, the aspect ratio or number of switching devices can be changed to improve the time.

| Transmission Gate Macrocell Simulation Results (VCC = 5V; 27°C) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Units** |
| $t_{ON1}$ | Turn On Time (to 10%; 2 pF Load) | | 3 | | nS |
| $t_{R1}$ | Rise Time (10% to 90%; 2 pF Load) | | 20 | | nS |
| $t_{OFF1}$ | Turn Off Time (to 90%; 2 pF Load) | | 3 | | nS |
| $t_{F1}$ | Fall Time (90% to 10%; 2 pF Load) | | 9 | | nS |
| $r_{ON1}$ | N-Channel On Resistance | | 2 | | kΩ |
| $r_{ON2}$ | P-Channel On Resistance | | 4.5 | | kΩ |
| $r_{OFF}$ | Off Resistance | | $5x10^{15}$ | | Ω |
| $Q_I$ | Injected Charge | | 4 | | fC |
| $I_{L4}$ | Leakage Current | | <1 | | fA |
| $I_{L5}$ | Leakage Current @ -40°C | | <1 | | fA |
| $I_{L6}$ | Leakage Current @ 85°C | | 112 | | fA |
| $V_{CC1}$ | Supply Voltage Range | 1 | | | V |
| $PSR_1$ | Supply Noise Rejection | | 52.4 dB | | V/V |
| $ICC_1$ | Supply Current | | <<10 | | fA |

**Table 4.3** Transmission Gate Simulation Data

Injected charge into a 2 pF capacitor results in a voltage change of 2 mV. The approximate sensor scaling is expected to be on the order of 1 psi/mV. Symmetric switching of both legs of the capacitors should cause this effect to appear as twice the frequency of the output voltage allowing the charge induced offset voltage to be removed from the signal.

The leakage current at 85°C will charge a 2 pF capacitor 1 mV in 17.9 ms. This would limit the minimum control frequency to be on the order of 28 Hz (twice this time interval). The operating frequency should be well above this value in order to minimize 1/F noise.

The supply related characteristics are all consistent with low voltage and battery operated requirements. All of this device's parameters are well within operating requirements, and there

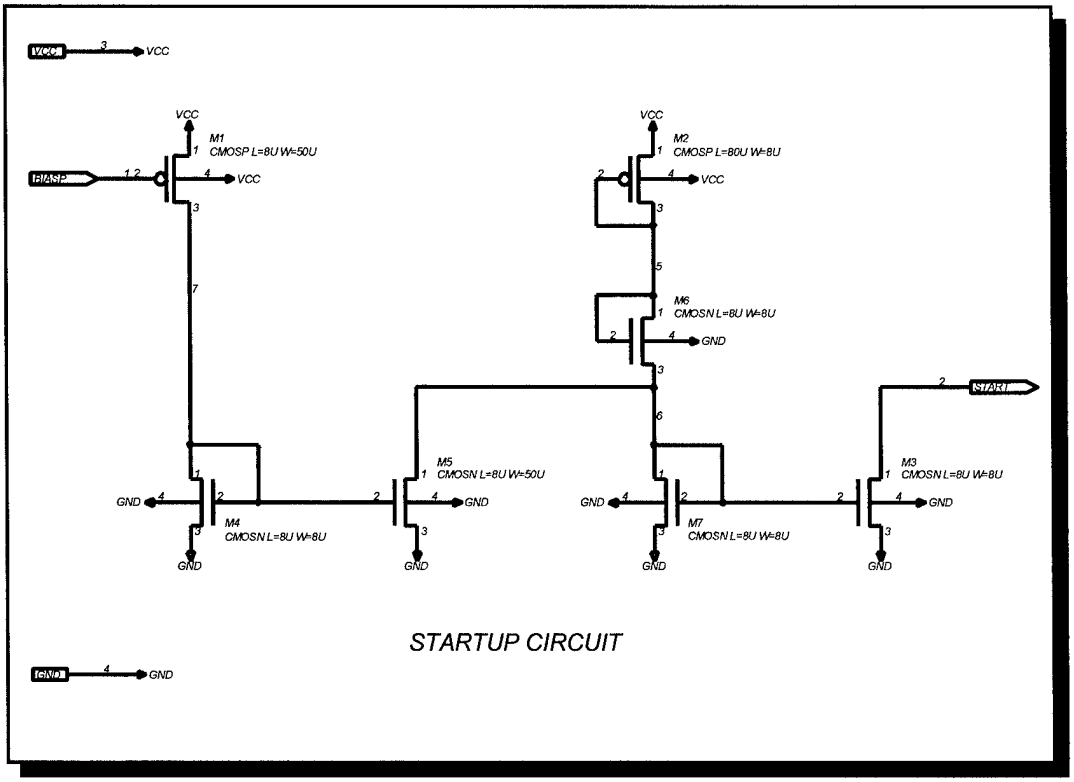


**Figure 4.15** Startup Macrocell Schematic

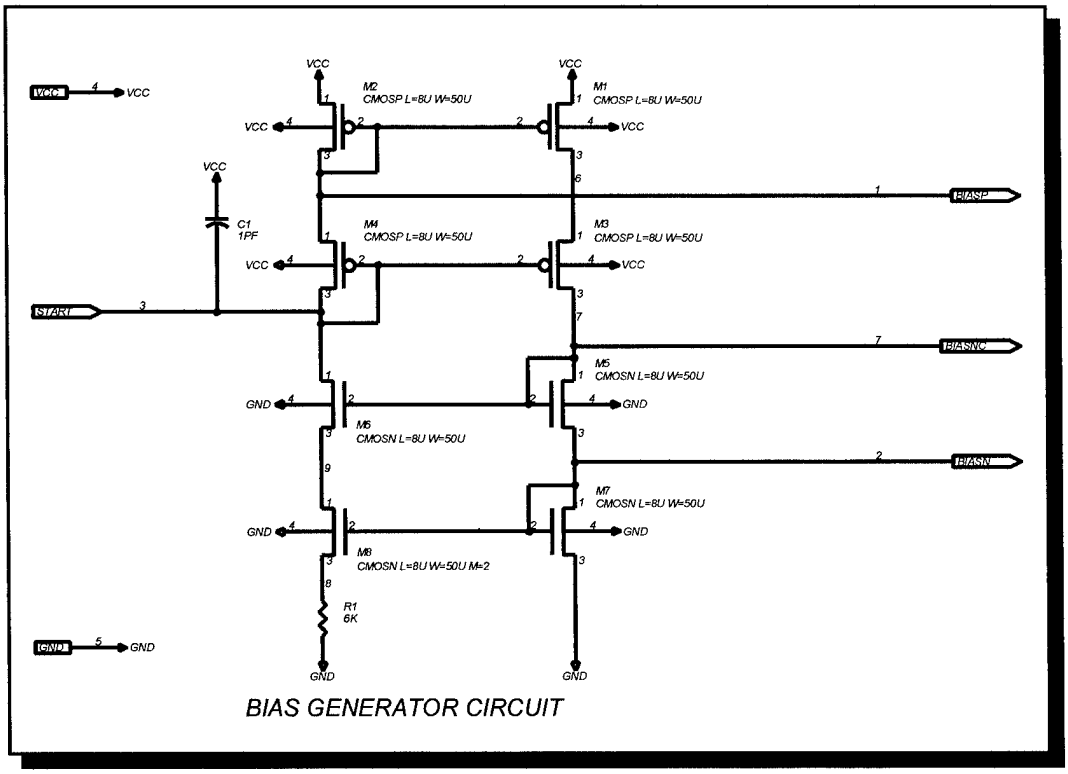


**Figure 4.16** Bias Generator Macrocell Schematic

are no significant issues related to the macrocell operation or usability in the fully integrated sensor.

#### *4.3.2.1.3 Startup Macrocell*

Figure 4.15 provides a schematic for the startup macrocell. This module is a new design to alleviate a potential problem in the bias generator macrocell, failure to start or slow to start.

Transistor M1 mirrors the bias generator current from the gate of an identical geometry transistor. Current mirror M4 and M5 amplifies the current by a factor of six, pulling current from the current source made up of M2 and M6. When M5 draws all of the M6 current, no current is available at the output transistor M3. M3 draws its current back from the bias generator. Because the nominal bias generator current is larger than the startup circuit M5 and M6 current, the startup circuit does not contribute to operating bias current.

Table 4.4 tabulates the results of TSPICE simulations for the startup macrocell for performance parameters.

This circuit provides adequate operation at 5V for the test chip but will require revision if applied to the fully integrated MEMS sensor. Revisions should reduce the supply current and minimum voltage requirements. These should be easily accomplished with the addition of more transistor devices and optimization of operating points for the supply requirements.

#### *4.3.2.1.4 Bias Generator Macrocell*

Figure 4.16 provides a schematic for the bias generator macrocell. The operating point of the circuit is set where the drain current of M7 is equal to the drain current of M8. The voltage drop across the dincrease the output resistance of the circuits and thereby improve the power supply rejection ratio of the bias generator current. This design is based on a Tanner macrocell with the addition of the cascode transistors.

Table 4.5 tabulates the results of TSPICE simulations for the bias generator macrocell for performance parameters.

**Startup Macrocell Simulation Results**
**(VCC = 5V; 27°C)**

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $I_S$ | Startup Current | | 160 | | nA |
| $I_T$ | Input Threshold ($I^O$ = .1 $I^S$) | | 180 | | nA |
| $VCC_2$ | Supply Voltage Range | 3.25 | | | V |
| $ICC_2$ | Supply Current | | 16.1 | | uA |

**Table 4.4** Startup Macrocell Simulation Data

| Bias Generator Macrocell Simulation Results (VCC = 5V; 27°C) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Units** |
| $I_{O3}$ | Output Current | | 11.1 | | uA |
| $VCC_3$ | Supply Voltage Range | 3 | | | V |
| $PSR_3$ | Supply Noise Rejection | | 30 | | nA/V |
| $ICC_3$ | Supply Current | | 22.2 | | uA |

**Table 4.5** Bias Generator Macrocell Simulation Data

This circuit, based on a Tanner macrocell, provides adequate operation at 5V for the test chip but will require revision if applied to the full integrated MEMS sensor. This device supply current is considered excessive to produce a 1.5 uA bias in the op amp circuits. Revisions should reduce the supply current and minimum voltage requirements. This should be accomplished by using a larger source resistor and optimizing transistor geometries for the supply requirements. To reduce the minimum voltage requirements, it may be necessary to eliminate the n or p channel cascode transistors (or both). This provides reduced voltage requirements at the cost of increased supply sensitivity. Reducing the supply current should also allow lower operating voltage requirements.

#### *4.3.2.1.5 Bias Splitter Macrocell*

Figure 4.17 provides a schematic for the bias splitter macrocell. The input bias on M4 results in a drain current approximately one sixth of the current in the bias generator. This current is mirrored in transistors M1 and M2. Saturated transistors M3 and M6 provide appropriate bias voltages for cascode stages in the op amps. Table 4.6 tabulates the results of TSPICE simulations for the bias splitter macrocell for performance parameters.

This circuit, based on a Tanner macrocell with added cascode stages, provides adequate operation at 5V for the test chip but may require revision the final MEMS device requires single 1.5V battery operation. The minimum supply voltage requirement can be reduced by reducing the bias current or eliminating cascode stages which improve supply rejection.

#### *4.3.2.1.6 Op Amp/Comparator Macrocell*

Figure 4.18 provides a schematic for the op amp/ comparator macrocell. This is a single gain stage design with a wide common mode input range with an effective rail-to-rail output swing. This circuit schematic is directly from a Tanner macrocell. This is a single stage op amp design where input differential amplifier M2 and M3 provides gain for signals near the ground rail and diff amp M9 and M10 provides gain for signals near the positive rail. The outputs of the diff

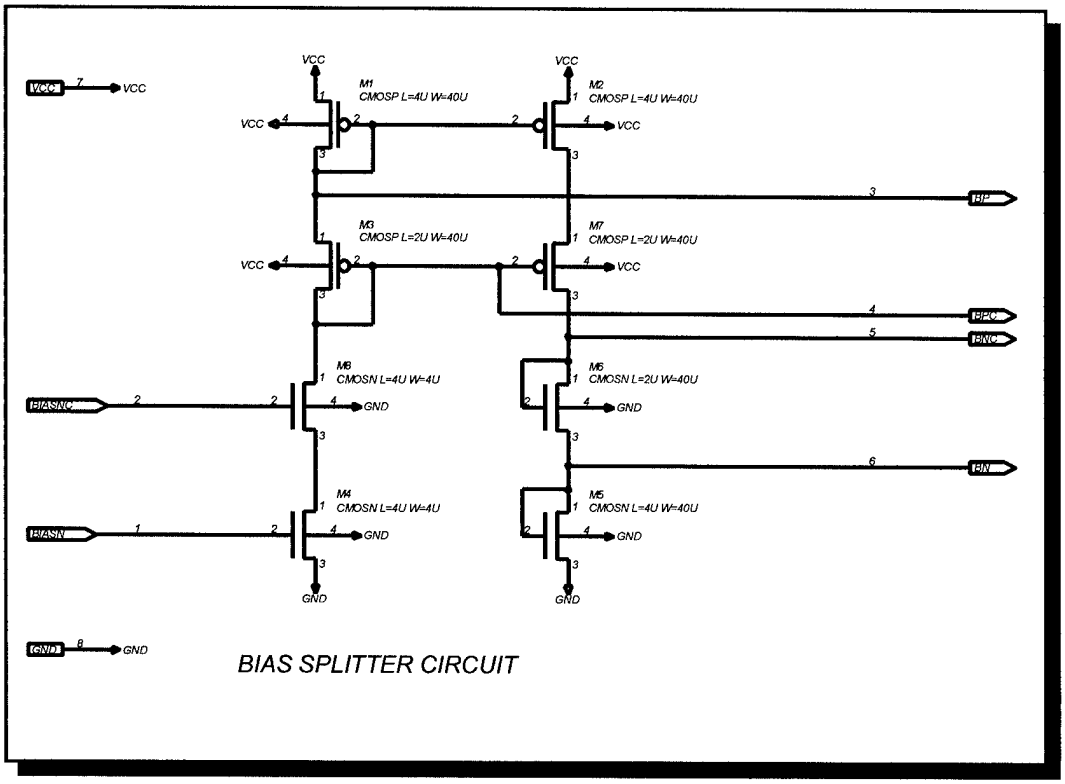


**Figure 4.17** Bias Splitter Macrocell Schematic

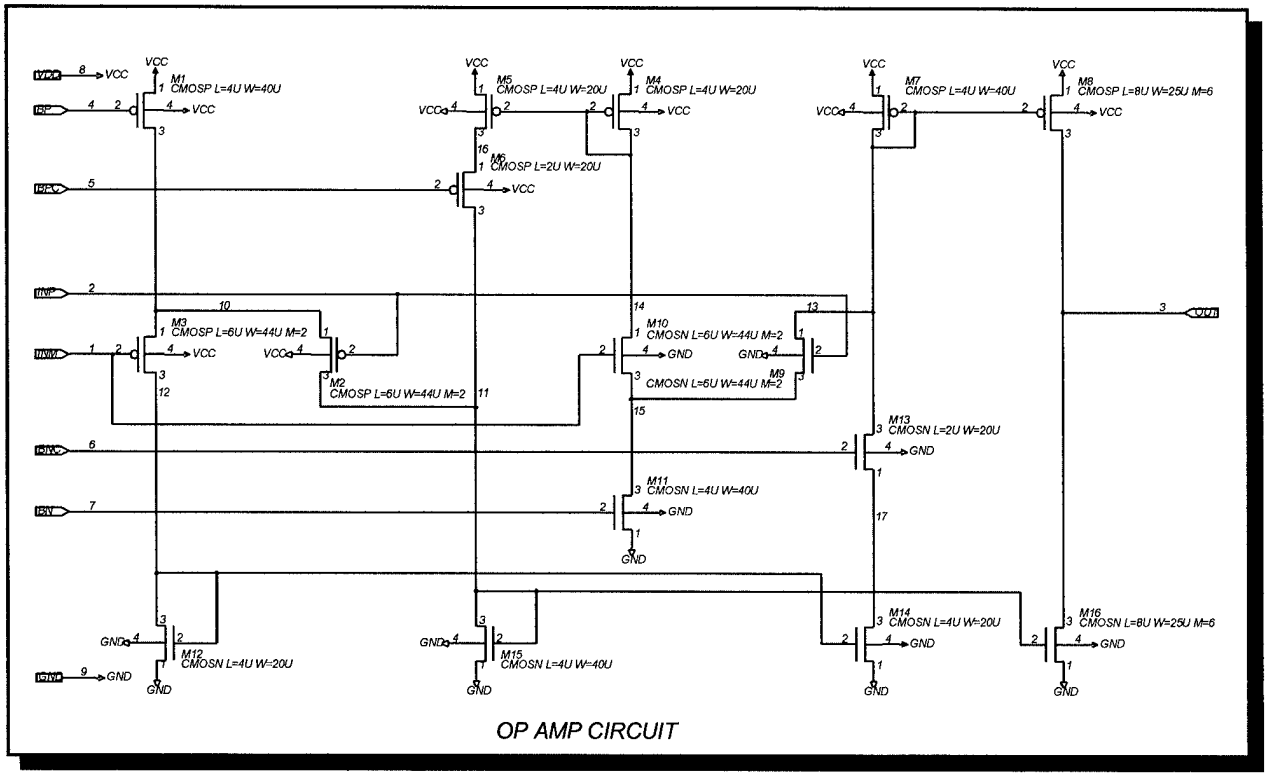


**Figure 4.18** Op Amp/Comparator Macrocell Schematic

| Bias Splitter Macrocell Simulation Results (VCC = 5V; 27°C) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Units** |
| $I_{O4}$ | Output Current | | 1.5 | | uA |
| $VCC_4$ | Supply Voltage Range | 2.5 | | | V |
| $PSR_4$ | Supply Noise Rejection | | 2 | | nA/V |
| $ICC_4$ | Supply Current | | 2.9 | | uA |

**Table 4.6** Bias Splitter Macrocell Simulation Data

amps are summed through current mirrors which apply the current to the output through a series of current mirrors.

The single stage op amp design exhibits excellent stability, but not a very high open loop gain. Open loop gain is primarily important in the charge redistribution capacitance measurement approach where the op amp is operated as a comparator where an additional gain stage would be required to provide a 5V swing from a signal below about 20 mV (~20 psi). For the test chip, this additional gain stage will be external to the integrated circuit.

The common mode input range and the output voltage swing allow test chip operation with signals approaching the supply rails. Note that the linearity is significantly degraded within about 1V of the supply rails, with input offset voltage increasing to as much as 40 mV.

The unity gain closed loop bandwidth limits the operating frequency upper limit for the device but should provide sufficient band width for sensor operation above the 1/F noise of the process.

Input offset voltage drift with temperature is not a very significant parameter since the AC drive of the capacitors will typically provide offset compensation.

Capacitive coupling of the supply to the capacitive sensor input contributes to the poor supply rejection of this op amp. For the test chip, the AC signal source is derived from the power supply so it is already important that supply noise be minimized. Low power supply noise is not inconsistent with a battery powered low current integrated design.

The supply voltage requirements and operating current are more than adequate for the test chip but may be further reduced with a reduced bias current level and eliminating cascode stages in the op amp.

The resistive and capacitive load capabilities are well within achievable external equipment and circuitry loads for the test chip. Reduced loading is anticipated for the final sensor since internal test points will most likely consist of probe pads and not leaded pins. This should also help achieve higher frequency operation if necessary.

**Op Amp/Comparator Macrocell Simulation Results**
**(VCC = 5V; 27°C; $C_{Load}$ = 15 pF; $R_{Load}$ = Infinite)**

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| AVOL | Open Loop Gain | | 48 | | dB |
| GBW | Gain Bandwidth | | 700 | | kHz |
| PM | Phase Margin | | 75 | | ° |
| GM | Gain Margin | | 23 | | dB |
| $V_{CM}$ | Common Mode Input Range | .04 | | 4.97 | V |
| $V_{O1}$ | Output Swing | 0 | | 5 | V |
| $V_{O2}$ | Output Swing $R_{Load}$ = 10 MΩ to Gnd | 0 | | 4.99 | V |
| $V_{O3}$ | Output Swing $R_{Load}$ = 1 MΩ to Gnd | 0 | | 4.68 | V |
| $BW_{CL}$ | Closed Loop Bandwidth | | 854 | | kHz |
| $V_{OS1}$ | Input Offset Voltage | | -7.6 | | mV |
| $V_{OS2}$ | Input Offset Voltage @ -40°C | | -11.7 | | mV |
| $V_{OS3}$ | Input Offset Voltage @ 85°C | | -5 | | mV |
| $PSR_5$ | Supply Noise Rejection | -23 dB | | | V/V |
| $ICC_5$ | Supply Current | | 6.6 | | uA |
| $R_L$ | Resistive Load | 1 | | | MegΩ |
| $C_L$ | Capacitive Load | | | 130 | pF |
| $t_{ON2}$ | Turn On Time (50 mV O.D.; 50 pF Load) | | 6.3 | | uS |
| $t_{R2}$ | Rise Time (50 mV O.D.; 50 pF Load) | | 66 | | uS |
| $t_{OFF2}$ | Turn Off Time (50 mV O.D.; 50 pF Load) | | 3.2 | | uS |
| $t_{F2}$ | Fall Time (50 mV O.D.; 50 pF Load) | | 43.9 | | uS |
| $VCC_5$ | Supply Voltage Range | 1.7 | | | V |

**Table 4.7** Op Amp/Comparator Macrocell Simulation Data

The large signal swing times limit the maximum operating frequency of the charge redistribution circuit. The reduced capacitive load associated with an internal circuit load would be expected to significantly increase the swing times in the full integrated sensor design. Table 4.7 summarizes the op amp or comparator characteristics as determined by simultation.

### *4.3.3 Test Chip Operation Analysis*

We also simulated the macrocells in capacitance measuring operation according to the test chip schematic (refer back to Figure 4.12) to demonstrate the operation of the test chip. The simulation also generates a set of electronic circuit parameters for comparison with bench top test ing of the test chips.Figure 4.19 shows the expected waveform for a .0244 pF capacitance difference operated in the integrated bridge configuration. This operation is commanded by DC restoring the common terminal to ½ the supply voltage and then applying a balanced drive from $V_{CC}$ to the sense and reference capacitors using transmission gates T1 - T4. The initial DC restore can be done with either T1 and T4 on or T2 and T3 on. Connecting the $V_{REF}$ pin to $V_{CC}$ forces the comparator output to high. The waveform after the DC restore shows a square wave amplitude of 23.78 mV pk-pk. This signal level corresponds to about 25 psia pressure. The voltage gain calculated from equation 13 for this case is 30.5 mV. The observed reduced gain is due to stray capacitance (capacitors, Figure 4.12, shown to $V_{CC}$ represent stray

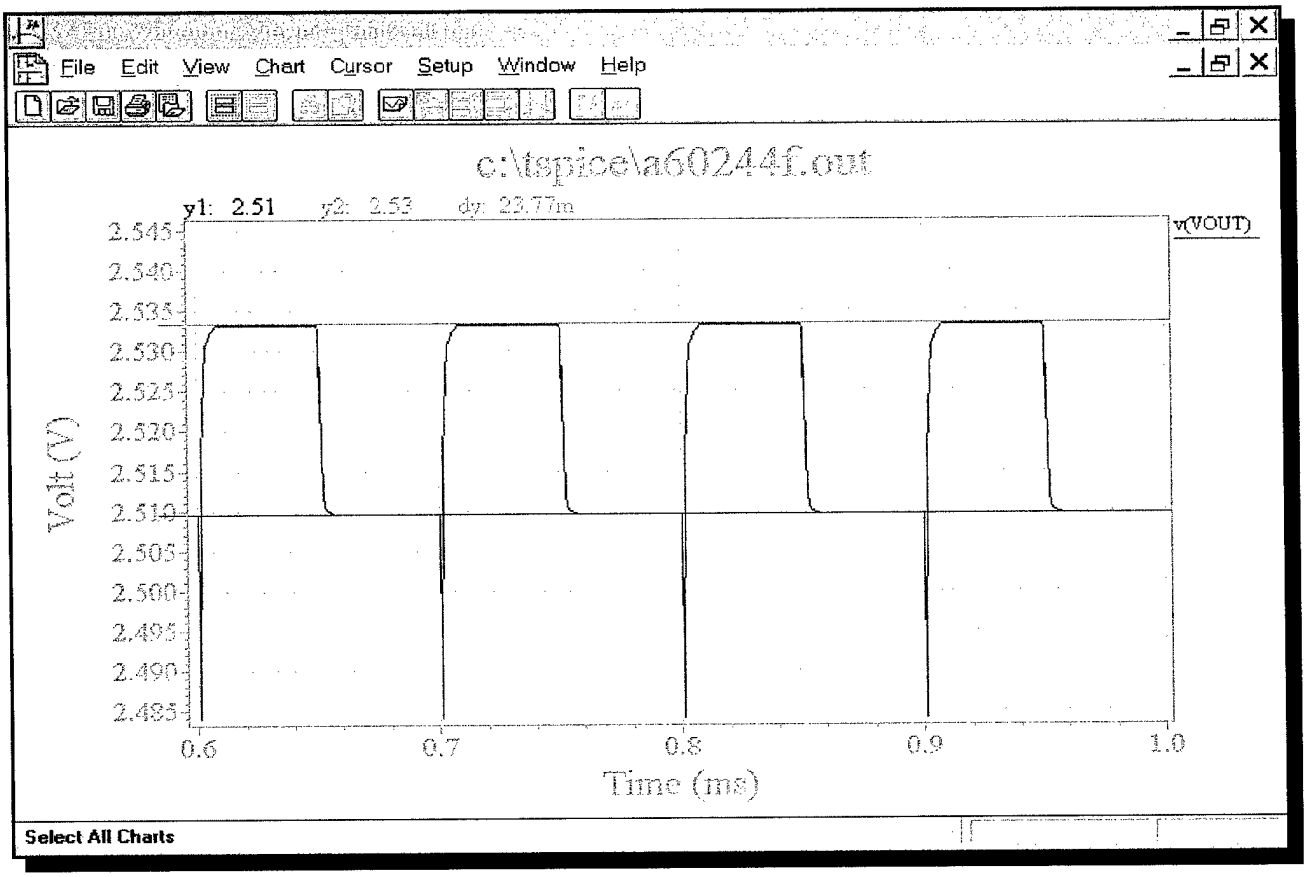


**Figure 4.19** Integrated Bridge Test Chip Simulation w/ 0.0244 pF Capacitance Difference

capacitances) loading the sensor output node through the feedback capacitor along with the gate capacitances of the op amps.

Connecting the comparator output to the internal feedback capacitance through transmission gate XSW6 obtains higher sensor signal swing with the same capacitance difference as shown in Figure 4.20. This is referred to as the high gain setting for the test chip. In order to DC restore this circuit, the comparator feedback is also applied to the VCM pin. The $V_{REF}$ pin is biased at ½ the supply voltage to establish the DC restore level through the amplifier feedback, first with XSW4 closed, then with XSW4 open. The waveform shows DC restore in both AC drive states. The effect is to double the signal amplitude.

Figure 4.21 shows the operation of the test chip as a charge redistribution system. The waveform labeled v(VOUT) in the legend of the figure shows the difference signal applied to a comparator (for example U1, Figure 4.11). The comparator output v(DOUT) connects to a simulated successive approximation register which drives a digital to analog converter (DAC). The DAC connects to the $V_{FDBK}$ and $V_{CC}$ test chip pads. In the figure v(FDBK) shows the resulting inverted ouput of the DAC (e.g., code $00_{16}$ = 5 V and $FF0_{16}$ = 0 V). The initial DC restore is performed with the DAC set to ½ $V_{CC}$ and the

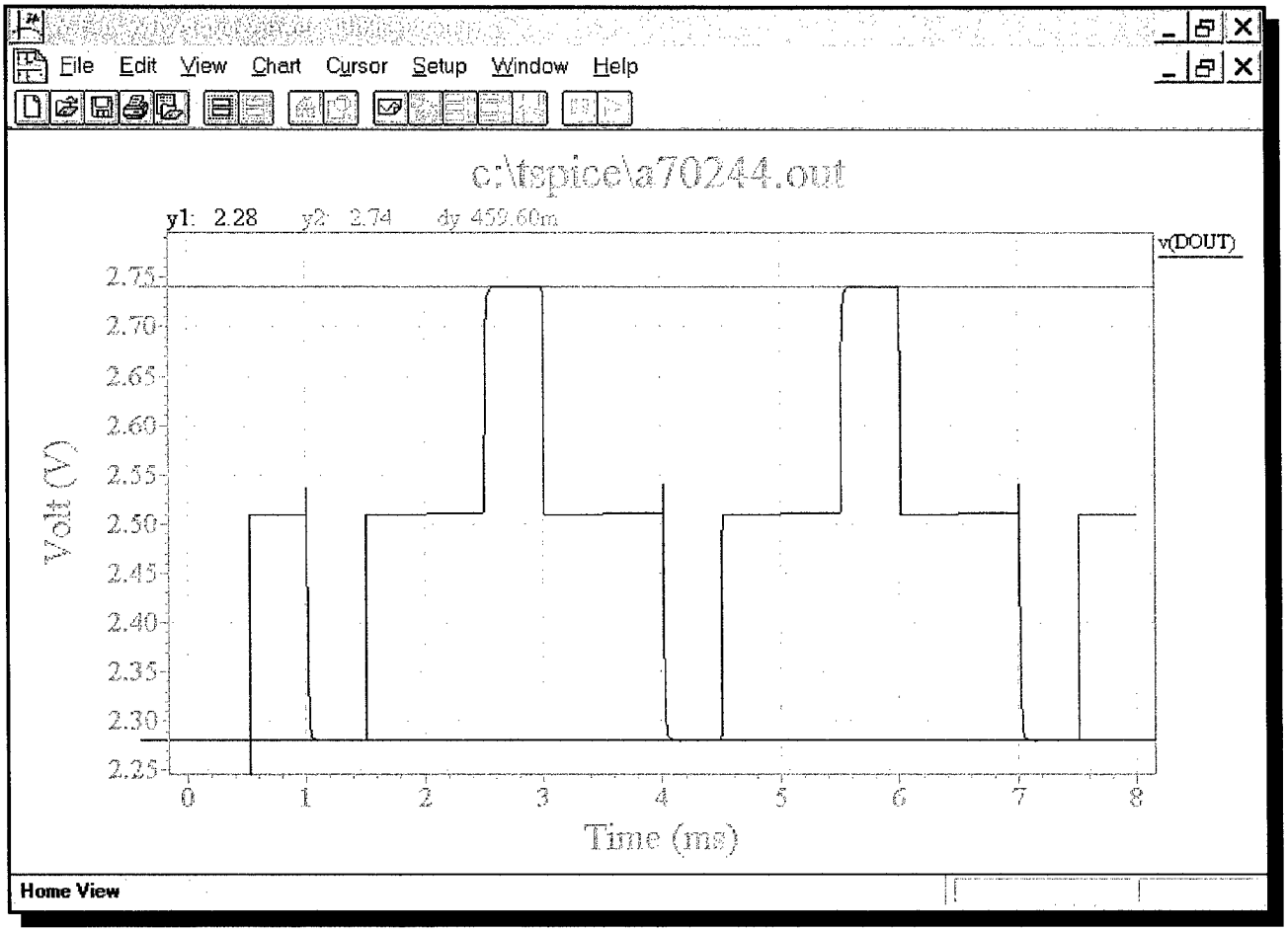


**Figure 4.20** Test Chip Simulation with .0244 pF Capacitance Difference and Internal Gain

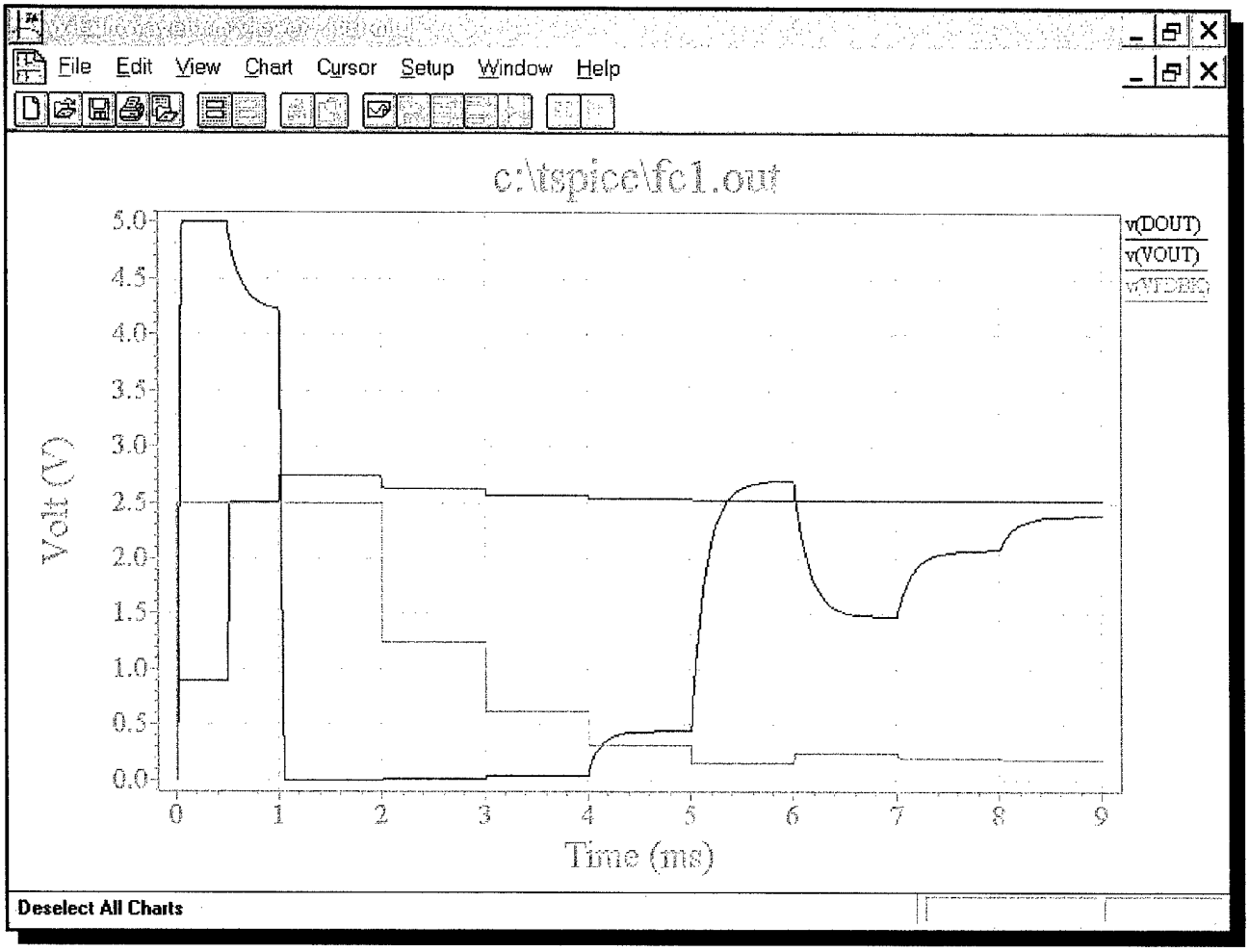


**Figure 4.21** Charge Redistribution Simulation of 8-bit ADC with 0.244 pF Capacitance Difference

feedback capacitor shorted out then released. The first bit decision with code $80_{16}$ = 2.5 V applied is low. The digital output is given by the comparator output within 1 msec. The DAC is then reduced to 1/4 $V_{CC}$ (code $C0_{16}$) and 1 msec later the next decision is registered. The waveform shows an eight bit sequence of codes which converge on the correct value $F7_{16}$. The simulated capacitance is nearly the maximum difference of .244 pF or approximately 250 psia.

Appendix B contains the simulation listings for these three different test chip operations. Table 4.8 tabulates the results of TSPICE simulations for the test chip operation in terms of integrated bridge capacitance measurement and charge redistribution capacitance measurement.

The high gain setting is approximately 20 times the unity gain setting. This reflects the maximum signal swing where the DC restore occurs during both phases of balanced AC drive. The higher gain operation reduces the bandwidth of the output amplifier and imposes lower operating frequencies of the AC drive.

Output offset was negligible as long as the drive is balanced and periodic. Switching spikes and offset due to charge injection then occurs at twice the signal frequency and is presumed to be removed by external analog synchrous demodulation or digital processing.

| Test Chip Operation Simulation Results (VCC = 5V; 27°C; $C_{Load}$ = 50 pF; $R_{Load}$ = Infinite) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Units** |
| **INTEGRATED BRIDGE CAPACITANCE MEASUREMENT** | | | | | |
| $F_{D1}$ | Drive Frequency Range Unity Gain | <.01 | 10 | 100 | kHz |
| $F_{D2}$ | Drive Frequency Range High Gain | <.01 | 5 | 10 | kHz |
| $A_6$ | Sensor Gain with Unity Gain Op Amp | | .0195 | | V/%C |
| $A_7$ | Sensor Gain with High Gain Op Amp | | .38 | | V/%C |
| $V_{OO6}$ | Output Offset | | 0 | | V |
| $VCC_6$ | Supply Voltage Range | 3 | | | V |
| $ICC_6$ | Supply Current Unity Gain | | 64 | | uA |
| $ICC_6$ | Supply Current High Gain | | 67 | | uA |
| $e_{N6}$ | Noise Voltage Unity Gain (.001 - 1 MHz) | | 21 | | uV |
| $e_{N7}$ | Noise Voltage High Gain (.1 - 10 kHz) | | 34 | | uV |
| **CHARGE REDISTRIBUTION CAPACITANCE MEASUREMENT** | | | | | |
| $F_{FDBK}$ | Feedback Frequency Range | <.01 | 5 | 1 | kHz |
| $A_8$ | Gain | | .19 | | V/%C |
| $e_{N8}$ | Noise Voltage (100 Hz - 10 kHz; Comp) | | 340 | | uV |

**Table 4.8** Test Chip Operation Simulation Data

The supply voltage range and current results show adequate performance for 5V operation of the test chip. Power dissipation at 5V is well under 1 mW. For long term battery operation, the supply voltage requirement and the current will require reducing. Macrocell analysis of this chapter discussed the feasibility.

All noise voltages are significantly less than 1 psi (~ 1 mV unity gain; ~20 mV high gain) which is considered adequate for the test chip.

Charge redistribution requires a long sample time due to the slew rate of the comparator. This can be reduced by reducing the capacitive load on the comparator. In the fully integrated MEMS sensor, this output would not be provided external to the IC and the capacitive load would be greatly reduced.

These chip level simulations show that the MEMS sensor can be interfaced to standard CMOS integrated circuitry and properly oper-

operated. To minimize the design effort and test chip risk, we used Tanner macrocells as much as possible. Future integrated sensors will require significant design revisions and redesigns to achieve all performance requirements, especially low voltage, long life, battery operation.

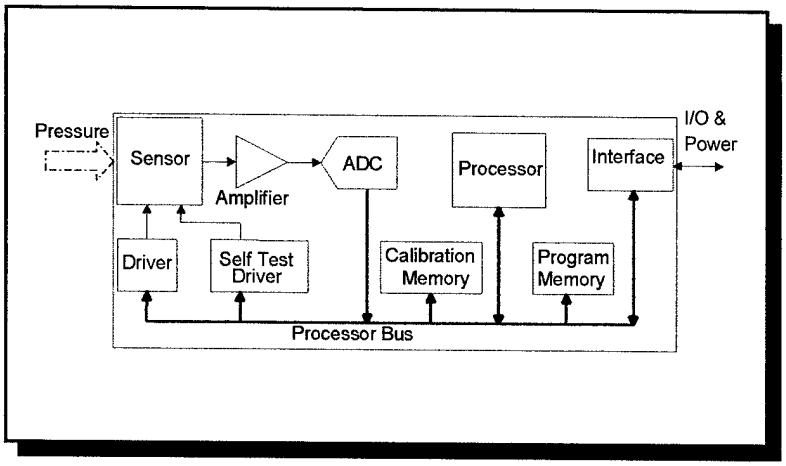


**Figure 4.22** Sure✓™ Integrated Sensor Conceptual Block Diagram

### 4.3.4 Allocated Digital Functions

Custom digital design in CMOS is more automated and better supported than analog or mixed signal design. Scalable designs exist for microprocessors and common interfaces, particularly those that are used in consumer computers. Considering the digital electronics functions to be lower risk than analog processing, this investigation considered only the allocation of circuit functions to the requirements.

#### 4.3.4.1 Integrated Circuit Block Diagram

Figure 4.22 presents a high level conceptual block diagram of the elements that are to be integrated into the sensor integrated circuit. Descriptive remarks for each block provide an overview of its function. All of these circuitry blocks are compatible with integration on a single CMOS device using standard fabrication. The normal CMOS passivating layers will provide protection of circuit transistors and interconnections during wafer post-processing steps previously discussed.

*Sensor* The sensor is either a piezoresistive or capacitive pressure sensor and a temperature sensor. Sensitivity, responsivity, and noise characteristics determine performance of system.

*Drive Circuit* The drive circuit provides the AC signal in the case of the capacitive sensor or DC biasing in the case of the piezoresistive wheatstone bridge.

*Self-Test Circuit* Consists of switches, references, and/or Coulumb force drivers to simulate "apparent pressure" self-test stimulus and assist in-use device calibration.

*Amplifier* Analog processing and conversion of sensor signals from low-level to ADC compatible level. Amplification, level shifting, differential to single ended conversion, and anti-aliasing functions are follow in importance to sensor characteristics for determining system performance.

*ADC* ADC (partially implemented by digital processor block algorithms) is a 10 to 12 bit sigma-delta converter employing tbd-bit feedback in oversampled conversion. Sigma-delta methods minimize anti-aliasing filter requirements of the amplifier.

*Processor* An 8 to 12 bit minimized special purpose digital processor with primitive DSP capability is required. Address and

data bus drivers for only on-chip ROM/RAM and I/O are needed. Clock management reduces power in standby and sleep modes.

*Program Memory* Approximately 2 to 4 kbytes ROM memory for operating program, and 256 bytes RAM, all low powerare needed. External ROM/RAM interfaces are needed only in oversized test devices. Separate test drivers reduces power and minimizes final chip area to fit.

*Coefficient Memory* Compensation coefficients in external EEPROM memory serially loaded to RAM by processor provides initial factory calibration and, as needed, fielded re-calibration of the Sure✔™ sensors.

*I/O and Power Interface* Approximately eight input/output, including power, signals interface with transponder subsystem. Manchester bi-phase encoded modulation performs data I/O communication with minimum pins. Power/GND separated after interface to separate analog and digital distribuitions to minimize supply noise.

### 4.3.4.2 Digital Processor Allocations

The processor provides digital filtering of the ADC output, conversion of the sensor output to a pressure reading (using stored compensation coefficients), I/O response, and control of the overall IC device. There are least two feasible alternative digital design implementations. Each is capable of meeting the prescribed signal processing requirements. Data sheets for candidate core designs include specifications for operating supply voltage down to 1.5V.

#### 4.3.4.2.1 VHDL 6502 Core

The first alternative is an intellectual property core design (e.g., the Western Design or V Automation 6502 core). This 8-bit microprocessor was originally developed by Rockwell. Its most well-known application was the N-MOS version used in the Apple II series and Commodor 64 personal computers. Rockwell has longed used the 6502 as a reduced instruction set (RISC) DSP in modems and, recently, in digital sequence direct synthesis wireless DSP chip sets introduced in 1996. Western Digital was founded by the original 6502 design engineer and the company's revenue comes mostly from 6502 products and intellectual property licenses. V Automation also makes the core available in synthesizable, scalable VHDL and as "hard core" GDSII layouts. The V Automation VHDL core is implementable as a "soft core" standard cell without separate license when implementing functions in Altera FPGA products. When used this way, it is a "black box" with internal detail hidden. The Encore! gate array conversion program also implements the 6502 core in its 1.2 μm and 0.8 μm CMOS lines.

The 6502 design, not including memory functions, is approximately 3500 CMOS gates. In 1.2 μm implementation the 6502 core is 100 x 120 mils (2.54mm x 3.05mm) a total area of 7.74 $mm^2$. Total allocated area of the digital processor function is 9.43 $mm^2$ on the integrated sensor IC. However, the area is contained in a shape consisting of a rectangle with an attached trapezoid. Approximate dimensions are 5.5 mm x 1.8 mm (rectangle), 1.8 mm / 1.5 mm (trapeziod bases), and 1.9 mm (trapeziod height). A challenge exists in refitting the core to the available geometry. External ROM/RAM memory interfaces (i.e., large, multiple address and data buffers) are not required except in the debug mode. Some silicon real estate may be saved by down scaling on-chip buffer transistor size to on-

chip bus fanouts, while providing parallel buffers of normal size to service the external test and debug interfaces. Although this may ease the design somewhat, it is not expected to enable the implementation in 2.0 μm process. Note that although previous analog analyses considered only a 2.0 μm process, the Orbit 1.2 μm is considered good for mixed signal design. The Orbit 1.2 μm process has all poly and metal layers which are needed for capacitive sensor implementation.

Firmware development for 6502 code has a natural test bed capability provided by the existing commercial products (samples have already been provided). Although not common, 6502 cross assemblers and C+ compiliers are available. Apple II or Commodore 65 computers would also make low cost and functional firmware development stations.

#### *4.3.4.2.2 Reverse Engineer CCM*

Another alternative for a digital processor is an early special function digital processor design (Widner,'82). This design, implemented in LS/TTL, was a 12 bit digital control module for multi-channel resolver signal analog to digital conversion. It was proven reliable on the AN/AAS-38 FLIR program.

The processor, or Converter Control Module (CCM), centers around a 12-bit arithmetic/logic unit (ALU) and two 12-bit ALU registers. Separate program (<1 k words) and data (<32 words/ conversion channel) memories each had dedicated busses. The CCM operated as a fixed point digital filter with two integrations in the completely digital processing loop. It controlled multiplexing and analog processing of 4 to 8 dual-speed resolver (Rx) input channels. Interfaces between the CCM and Rx multiplexer were channel and speed select, 14-bit feedback angle (sin/cos multiplying DAC) and 8-bit Rx/feedback difference (loop error). Outputs of the CCM were 16-bit resolver angle (although 24-bits were calculated by CCM), 16-bit resolver angular rate, a built-in-test signals consisting of converter status (8-bit) and loop error signal (proportional to angular acceleration). Digital filter iteration rates were 6400 Hz for a loop error demodulator and 800 Hz for main loop processing.

Partial design documentation was retained and engineering drawings are available. Upon comparing resolver converter function and the charge redistribution process, it is evident that CCM is adequate for the signal processing needs of this application. The design if converted to CMOS is estimated to be less than 2000 gates. Estimated silicon area required is 9.2 $mm^2$ or less.

Conversion of this early design into 2.0 μm CMOS represents a similar situation to converting the 6502 to the new form factor – significant layout work is required but reverse engineering is also required. Starting with schematic diagrams and a functional knowledge of the circuit, a reverse engineering first step converts the design LS/TTL to CMOS FPGA logic. The implementation must follow a rule set which will ensure suitability for conversion to a 2.0μm N-well double-poly, double-metal process. The output schematics, net lists and VHDL database provide a verification means through simulation. The final steps in the design validation are to implement the VHDL design in an FPGA including firmware code. Pre-silicon step integration and testing are the same as for the 6502 core. Although, fewer software programming tools exist for this processor than for commercial integrated circuit processors, the algorithm needed is short and simple.

Primary differences in the designs are in level of maturity of their implementation in the selected

CMOS process and in their gate count and functionality.

### *4.4 Mechanical Design Simulations/Analysis*

Analysis of the design included a finite element model of the metal barrel and integrated circuit assembly using Pro/Mechanica FEA Software. The structure was subjected to Thermal and Pressure loading. The subcontractor's report is included as Appendix A. Four separate load cases were analyzed. A strength analysis of the IC, Barrel (package) and bond line interfaces were performed. The mechanical response of the Silicon Membrane was analyzed.

### *4.4.1 Summary of FEA*

The Model consists of three major parts:

(1) The barrel consists of a kovar tube containing a slit. The barrel to the right of the slit is depressed forming a window and a shelf.

(2) The IC (silicon) is located through the window and it interfaces both on the inside of the barrel and the outside of the barrel on the shelf. The exposed portion of the IC has features defining a thin membrane over a evacuated chamber (pressure transducer).

(3) The epoxy bond lines are modeled as .025 mm (.001") thick. These elements connect the IC to the barrel.

Table 4.9 shows the four load cases that were analyzed. For all analyses the stress free temperature was assumed 150°C, the cure temperature of the epoxy bond lines.

For the kovar and silicon, the factor of safety used was 1.2. Because of the uncertainty inherent in adhesive bond line stresses, the factor of safety used there was 1.4. Using the method explained in Appendix A, an acceptable strength criteria is a margin of safety greater than zero.

| | PRESSURE | TEMPERATURE |
|---|---|---|
| CASE 1 | 0.000 N/mm$^2$ | 25° C |
| CASE 2 | 5.512 N/mm$^2$ | 25° C |
| CASE 3 | 5.512 N/mm$^2$ | 200° C |
| CASE 4 | 5.512 N/mm$^2$ | -55° C |

Table 4.9 **Load Conditions Analyzed**

### *4.4.2 FEA Results*

Figures in Appendix A show the stress concentration for all analysis conditions. Table 4.10 provides summary data of worst case conditions. The analysis reports high margins of safety for the barrel and IC. The structural integrity of these components should be of little concern.

However, the margins of safety on the bond lines are small. Therefore the structural integrity is marginal. The analysis recommended design modifications to reduce the bond line stresses and a more thorough investigation of the bond line by analysis and test. This investigation analyzed two components of shear stresses on the top and bottom bond lines. The two shear stress components were vector summed and reported in Table 4.10. Significant items are peak stress of 6.4 Mpa (MoS=.21) for the top bond line and peak value of 16.9 Mpa (MoS=.02) for the bottom bond line. These stresses are caused by at least two factors. First, the epoxy adhesive has a much larger coefficient of temperature expansion (CTE) than the barrel or IC. At -55°C the bond line thickness shrinks relative to the barrel and IC. Then, because the IC is

bonded on both surfaces, both bond lines are put in tension. The shelf is a compliant portion of the structure. The pressure loads on the shelf are transferred to the barrel through the IC, also putting the bond line in tension.

Although all safety margins are positive, the relatively high bond line stresses are a cause of some concern for several reasons:

(1) The allowable stress values for bond lines are estimates. Epoxy bond strengths aredependent on many factors, such as tem perature, surface preparation, surface chemistry and processing.

(2) The failure criteria used does not consider the combined shearing and tensile stresses and the nonlinear nature of bond line stresses.

### *4.5 Commercialization Factors*

Although the interest in improving tire pressure measurement has been high for many years, the technology is just now available to economically

| NOVEL PACKAGE AND IC STRENGTH ANALYSIS | | | | | |
|---|---|---|---|---|---|
| **STRESS (MPa)** | **LOAD CASE** | | | | |
| | **1** | **2** | **3** | **4** | **Allow-able specifi-cation** |
| | 25 'C 0 PSI | 25 'C 800 PSI | 200 'C 800 PSI | -55 'C 800 PSI | |
| **KOVAR CASE** | | | | | |
| Von Mises Stress | 24 | 178 | 165 | 180 | 345 |
| *Margin Of Safety (1)* | **10.98** | **0.62** | **0.74** | **0.60** | |
| **SILICON IC** | | | | | |
| Max Prin Stress | 8.0 | 62.3 | 60.5 | 63.2 | 700 |
| *Margin Of Safety (1)* | **71.92** | **8.36** | **8.64** | **8.23** | |
| **TOP BOND LINE** | | | | | |
| Max Shear Stress | 0.5 | 4.5 | 3.7 | 6.1 | 10.35 |
| *Margin Of Safety (2)* | **12.73** | **0.66** | **1.00** | **0.21** | |
| Flat Wise Tension | 0.8 | 4.2 | 4.5 | 6.0 | 24.2 |
| *Margin Of Safety (2)* | **22.05** | **3.12** | **2.84** | **1.88** | |
| **BOTTOM BOND LINE** | | | | | |
| Max Shear Stress | 2.48 | 3.46 | 2.55 | 5.11 | 10.35 |
| *Margin Of Safety (2)* | **1.98** | **1.14** | **1.90** | **0.45** | |
| Flat Wise Tension | 2.70 | 12.6 | 9.6 | 16.89 | 24.2 |
| *Margin Of Safety (2)* | **5.40** | **0.37** | **0.80** | **0.02** | |

Table 4.10 **Summary of Worst Case Stresses from Finite Element Analysis**

meet an emerging market. Previous attempts were technically unacceptable or too expensive for mass consumer market feasibility. Anecdotal reports from many sources detail the extreme barriers to entry of new products and suppliers to the automotive sector.

The Detroit system expects R&D and production tooling expenses to be borne by suppliers before the decision makers are more than casually interested. The Epic Technologies, Inc. system now optionally available on the '96 Lincoln Continental saw seven lean years since its '89 availability on the Chevrolet Corvette. With such limited luxury consumer market niches, one might still suspect the market realism. Evidence to the contrary is presented in the next section which discusses two new marketable innovations that are on the horizon.

### 4.5.1 Near-term Market Innovators

The invention of a MEMS IC embedded in tire casing (Brown,'91) will likely be a success because, in addition to consumer features, there are advantages to the tire manufacturer with respect to product warranty logistics. These advantages and the relatively low added price to a consumer, practically eliminate market or economic barriers for this product.

Another product has enabled a Canadian company, UniComm *Signal*, Inc.(UniComm Signal,'96) to have a public offering of stock in the last few months. Their market entry plan was similar to RainTree Technology's plan for the Sure✔™ devices. Their product is retrofittable on car and truck wheels. It is a wireless encapsulated module which requires dismounting tires from rims for installation. The module, containing batteries with anticipated life of three years, straps onto the pressure side of the rim with an adjustable band tensioned around the inner circumference of the wheel. Initial steps to market were provided by the mining industry where the product was proven. The new TMS (standing for tire monitoring system) is an on-highway version of the product. The company claims that it has endorsement of major tire manufacturers and that it has production capability established in the U.S. and Japan. Company news releases claim the targeted market for TMS is 1% of vehicles. The U. S. production facility is expected to be on-line with a production rate of 250,000 devices per month by year end 1996. As this company demonstrated, a viable way to market for this technology is through after market and trucking fleet sales not via the automotive OEMs. UnicComm *Signal* recently announced the purchase of Epic Technologies Low Tire Warning Division.

### 4.5.2 Consumer Marketing Via Air Quality Programs

Motor vehicle registration in California includes a $2.00 per vehicle per year county assessment. The San Diego County Air Pollution Control District (SDAPCD) receives $3.8 million per year from this source of revenue. With these funds SDAPCD has established a program which funds programs to reduce pollution in San Diego county. The past funding for projects has exceeded $11 million. Projects which have been funded include purchase of alternative fueled busses for municipal districts, establishing bike lanes (including advertising funds) and scrapping of older, highly, polluting vehicles. One research and development project was funded to develop retrofit catalytic converters for older automobiles. The R&D program was followed with a funded program to subsidize the installation of the newer catalytic converters on qualifying vehicles.

RainTree Technology prepared a proposal to the

SDAPCD for R&D funds, and this is presently in review and evaluation. The next competitive cycle is in two years.

Data from University of Alberta and Alberta Department of Energy studies (UA,'92) have shown that significant savings in fuel (hence, pollution as well) are possible with improved tire pressure maintenance. From calculated emission reductions of a program involving aggressive county wide marketing, Sure✓™ promises larger potential impact than any previously funded SDAPCD program. Therefore, the SDAPCD program is a high priority candidate for first production sales of Sure✓™ as are other similar large government district programs. The plan is workable because, by not requiring tire removal, Sure✓™ will be easier to retrofit than other wheel mounted sensors (e.g., the TMS device). We also anticipate an invention review addressing marketing feasibility from the WalMart Innovation Network in the near term.

**Calculations - Estimated Future Emission Reduction**

| | grams/mi | *7.07 factor | *17.67 factor |
|---|---|---|---|
| ROG VMT (CA Air Res.,'95) | 0.57 | 4.03 | 10.07 |
| Nox VMT | 0.69 | 4.88 | 12.20 |
| CO VMT | 4.56 | 32.25 | 80.60 |
| **TOTAL EMISSION REDUCTION** | | 41.16 tons/year | 102.87 tons/year |

**ASSUMPTIONS**

San Diego county vehicles 1,900,000
Average yearly Vehicle Miles Traveled (VMT) is 13,000 miles/vehicle
Data reported in Alberta Audits apply to San Diego county vehicle population
2% to 8% range of reduction in fuel consumption is available by tire pressure improvement
average fuel consumption reduction available is 4.5% (actual implemented savings is 3%)
5/12 (42%) of owners are more conscientious in maintenance than the remaining 58%
Fuel consumption reduction % applies equally as reduction % in emission based upon grams/VMT
Conscientious owners are more likely to respond to tire pressure product (i.e., target market = 45%)
Long range market penetration is 25% of target market
Product installation during two-year category 1 or 2 project is 10% of target market

* Factor 7.07 tons/year converts g/mi for 79,800 vehicles implemented with APCD funds
* Factor 17.675 tons/year converts g/mi for 25% market penetration

Table 4.11 **Pollution Emission Factors for Implementing Tire Pressure Measurement**

# CHAPTER 5

# CONCLUDING REMARKS

# 5 Concluding Remarks

RainTree Technology obtained significant results with regard to the feasibility of implementing the Sure✔™ tire pressure measuring system. The highly integrated multi-discipline nature of the project required a tremendous amount of interdependent work. Designs of new packages, new sensor structures, modifications of prior corner compensations, electronic analog circuits, and silicon layouts were attempted. We faced a significant learning curve with new tool sets as well as learning the MEMS engineering discipline. With a few exceptions, which are still being worked, we accomplished the goals set out initially. Our conclusion of the study is that the approach is feasible technically and that a market has developed where the product would be viable economically. The following paragraphs summarize the availability of several promising technical approaches. Detailed conclusions with regard to the various study aspects follow in this chapter.

As presented in Chapter 3, the constraints on the design are severe but not insurmountable. There are extreme limits on chip size and packaging combined with stressful environmental conditions. We developed designs that pushed for highest performance in sensor dynamic range and sensitivity in order to make one product configuration fit all tire applications. The objective of this is for one configuration to maximize production quantity to reduce unit cost. Simultaneously with striving for the highest capability, we evaluated circuit designs that would achieve these ends in one of the simplest and most accessible CMOS processes (Orbit's 2μm N-Well technology) that is currently available. While this was favorable for analog circuits, it imposes restrictions on the number of gates which are implementable on the chip. This in turn narrows margins with respect to the floor plan of the chip and pushes the design to select anisotropic etching masks which are perhaps more complicated than would otherwise have been necessary. However, with respect to every trade off complicated by the factors relating to achieving wide-dynamic range, there is an acceptable fall-back implementation. Implementation of the mitigating options may in some cases dictate a lower performance sensor. In such cases a series of IC mask configurations can provide devices with overlapping pressure operating ranges. In other cases fall-back position may increase cost of development without necessitating abandoning a single configuration design.

The following subsections discuss first how the results obtained support our conclusions and recommendations. Next is a discussion of expected testing of designed circuits. Expected results are guided by fairly well-documented results from other researchers and by review comments from other experienced researchers. However, because the details matter greatly, there is a moderate risk that experiments will not go as predicted. We present the probable results and discuss the projected risks associated with these conditions in the second subsection.

## 5.1 Conclusions Supported by Results

An implementation methodology involving successive design iteration and test is feasible for further development of the Sure✔ product design. Figure 5.1 shows a high level flow process for this development, and the process is discussed in the following paragraphs.

### 5.1.1 Process Development Surface Micromachining

The design rules for the various IC processes were developed for reliable construction of electronic devices in integrated circuits. Except for pad bonding holes, all layers are generally

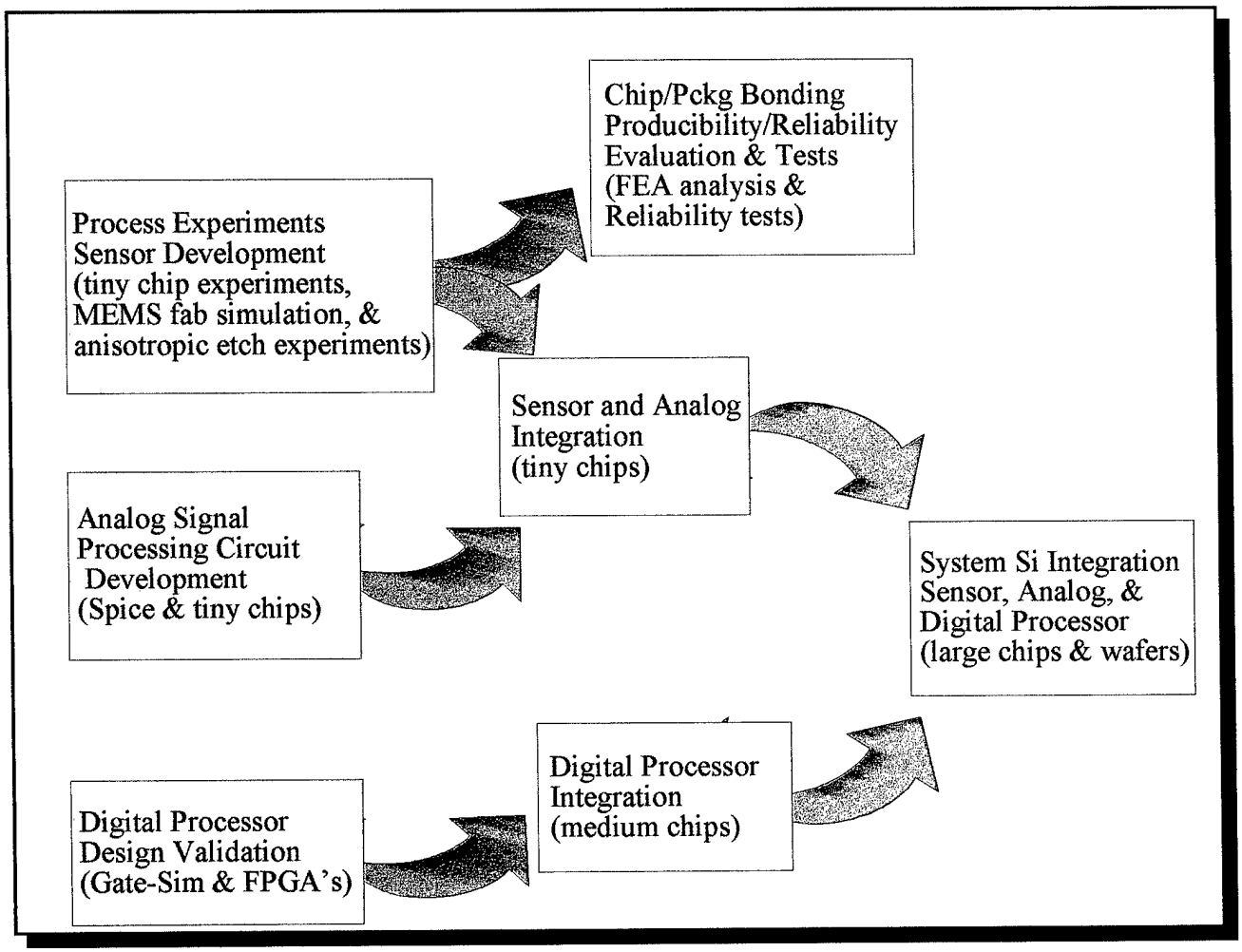


**Figure 5.1** Integrated Circuit Development Flow

covered with one or more oxide layers. In order to construct our three dimensional air gap capacitors and/or to release the diaphragm and establish a vacuum reference plenum, the mask set must violate certain CMOS design rules in the sensor area. These violations, which open lower layers (poly-silicon or oxides) to post-process access, also expose intermediate layers to the etching processes for upper oxide layer removal. These processes were not designed to stop or be selective against etching the lower layers. Indications are that past experience of other researchers using the MEMS rules in MOSIS has been variable and less repeatable than desired. Therefore, process experiments into the etching characteristics as they relate to our proposed non-standard stacking of contacts, vias, and over glass cuts are required. Experiments with multiple fabrication runs to determine etch rate, material selectivity, repeatability are necessary before the design and development can be expected to succeed. Foundry assistance will greatly expedite this characterization process. Proprietary agreements with the candidate production foundries to protect the foundry process and RainTree Technology's designs need to be negotiated. Then the development could work could include simulating process characteristics. Many more design trials are feasible using foun-

dry proprietary process data with one of the MEMS fabrication simulation tools.

### *5.1.2 Packaging and Anisotropic Etch Process Development*

Our finite element modeling showed a high degree of margin for structurally withstanding the pressure loads and temperature stresses that the product will experience. The modeling was conservative with respect to the geometries modeled. The highest stress condition occurred in a sharp corner which will not exist in the actual product. The next highest stresses were an order of magnitude lower. The design changes made in the barrel for two-step fabrication by screw machining/die stamping implement recommendations made by the analysis engineer. This should further increase margins in the area of greatest concern. On the other hand, the geometry changes introduced asymmetries and holes in the part. However, the modified barrel geometries occurred mainly in areas where stresses were relatively benign. Significant changes in wall thickness or new holes only occurred in an area which is not exposed to the pressure loads. There is little concern that results will change in a new finite element modeling analysis.

A more significant concern lies in the area of the adhesive bond interface. The model for this interface consisted of simple uniform planes and rectangular solids. With physical parts assembled in production, the interface will more likely comprise minor wedges, surface roughness, and voids. While not likely to upset the structural integrity of the sensor packaging (the surface areas are relatively large) the non-uniformities may cause strain gradients in the sensor substrates. Although we attempted to evaluate this via the finite element model, the displayed range for the output gave insufficient resolution to confidently evaluate the concerns. Additional finite element analysis incorporating the micro-detail of the sensor structure may be necessary. Boundary conditions for such a simulation should consist of results of a physically realistic bonding interface model. Variations of the parameters suggested above may provide useful data for evaluating calibration reliability. As discussed in Chapter 3, this is a user concern.

The results show that there is adequate margin in the available area for realizing the estimated circuits needed. Furthermore, the design accommodates spare area for growth in actual circuit vs estimated gate count. With regard to maximizing circuit area and implementing functional floor plans, we investigated compressed corner compensation designs and found several potentially suitable. In addition, less corner compensation is probably adequate in the design with modifications to the arrangement of the circuits and scribe lanes on the wafer.

### *5.1.3 Analog Signal Processing Development*

Our design, starting from macro-cell circuits, was successfully modeled using T-Spice. The initial T-Spice runs showed areas of deficiency with respect to this application. Redesign of the circuits provided improvements as shown by simulation. The redesigned/modified circuits have been implemented in mask layout for test circuits along with test sensors. Additional analog circuit development and improvement is needed. The analog processing circuits follow steps presented in Figure 5.1.

While process experiments/sensor design and digital processor portions of the chip are in development, custom silicon analog signal processing implementation can be pursued in a parallel path. Design iterations to characterize fabrication parameters for the sensor can be

implemented on the same or different IC's depending upon the level of maturity of the design elements. Additional (and presumed better) analog macro cell models are available from foundries for specific in-house processes. Rapid prototyping is available in MOSIS and Foresight programs for the Orbit 1.2μm and 2.0μm CMOS. Both are double poly, double metal processes (as required for our capacitor sensor approach) with good analog characteristics. There are also suitable BiCMOS processes available as potential alternatives available with known improvements in analog processing vs CMOS.

We showed that standard CMOS process provides the functions required to integrate the MEMS sensor to a digital processing system. We demonstrated this with the integrated electronic design for the MEMS test chip. There are, however, several challenges ahead for the electronic design of the fully integrated MEMS sensor. These challenges include achieving the necessary signal resolution within the process, especially on a mixed signal device; achieving satisfactory operation at low voltages and supply currents consistent with a sufficiently long- lived battery power supply; and providing a fully integrated high-yield design with sufficient accuracy and long- term stability.

### *5.1.4 Digital Processor Allocations*

At least two feasible alternative digital design implementations were presented, each capable of meeting the prescribed signal processing requirements. Primary differences in the designs are in level of maturity of their implementation in the selected CMOS process and in their gate count and functionality. While the area available is adequate for the 6502 core in its mature implementations in 0.8μm and 1.2μm CMOS, the "hard core" implementations from GDSII format are not useable. The high aspect ratio rectangle inherent in our design will require significant layout work to convert the approximately square cores. Scalable VHDL data to support such conversion is available as a starting point Tools for the design and scalable macro cell models are also available.

The process for implementing the 6502 design in a twin well double-poly, double-metal 1.2μm process begins at the bottom left of Figure 5.1. Design validation implements the design using sample kits (e.g., commercial 6502 parts in the target process) verifying functional performance of the design, second implement the VHDL core design via simulation, and then implement with an FPGA (e.g., Altera ) replacing the kit parts. These are functional and timing verification steps.

Another early digital processor design ( LS TTL implementation) has proved reliable on the AN/AAS-38 FLIR program. It is available and adequate for the signal processing needs of this application but needs to be converted to CMOS. Conversion of this early design into 2μm CMOS represents a similar situation to converting the 6502 to the new form factor – significant layout work is required but reverse engineering is also required. Starting with schematic diagrams and a functional knowledge of the circuit, the first step is to reverse engineer the design and convert from LS TTL to CMOS FPGA logic. The implementation must follow a rule set which will ensure suitability for conversion to a 2.0μm N-well double-poly, double-metal process. The output schematics, net lists and VHDL database provide a verification means through simulation. The final steps in the design validation are to implement the VHDL design in an FPGA including firmware code. Pre-silicon step integration and testing are the same as for the 6502 core. Although, fewer software programming tools exist for this processor than for commercial

integrated circuit processors, the algorithm needed is short and simple.

Finally, for either approach, converting proven designs for the FPGA implemented digital processor to custom silicon with required form factor can be accomplished with rapid prototyping in either 2.0μm or 1.2 μm processes from MOSIS and/or Foresight foundry process(es). In addition FPGA conversion services are readily available from a number of sources including Orbit, TMSC, and other foundries and also from service bureaus.

Success in design validation enables the integration of the digital electronics as a stand alone design in medium size chips employing the rectangular form factor. Only a few pins of I/O are needed for the final design with power distribution expected to be challenging. This issue alone may require rapid prototype iterations in spite of the norm for digital process integration being first pass success. The remaining many pins of a medium lead frame are available to be used as test points for the connection of debugging memory, I/O, and test probes. The digital processor core should receive power via the final I/O pins and test buffers should have separate power distribution.

### *5.1.5 Final Integration*

Final series of steps in sensor integration involve adding incrementally integrated and tested digital electronics, analog processor, sensor designs, and process recipes into one layout and fabrication process. Foundry standard large chips or user defined size (sold by cost/mm$^2$) are available. This is still using relatively low-cost multi-user foundry services for putting all the pieces together. For example, a large chip can contain three chips of the size needed for Sure✔. Final steps will validate the production process by purchase of complete wafers. These will yield sufficient chips to begin qualification and life-cycle testing.

## *5.2 Other Remarks - Expected Results and Risks*

The experiments that were designed have not yet been carried out. Several factors contributed. Proprietary information protection required more effort and, more importantly, turn around time than previously anticipated. Initial concepts for fabricating the barrel with deep draw metal stamping and/or high volume casting were rejected by suppliers. The issues cited were the Kovar material specification and the chip interface geometry. These were not inconsequential issues. Solving these problems generated many rounds of discussions, selection of alternate processes/vendors and redesign. As a consequence, time was directed away from a quicker completion of layout design of the test chip for MOSIS fabrication, thereby delaying implementation. The highly coupled form factor of the sensor chip with the barrel design required finalizing the interface of the barrel in a producible configuration. Although general experiments (e.g., corner compensation or CMOS process effect on open via, open metal) could have been continued, we chose a path directed at implementing the selected design alternatives.

### *5.2.1 Packaging and Micromachining*

Anisotropic etching is a necessary step in defining the shape of the sensor chip. Masks are complete for several options of the anisotropic etch sculpting of the sensor chip. The redesign associated with the barrel fabrication somewhat simplified the etching. Corner compensations need not be perfect in defining the shape drawn. Circuit layouts can adjust for inaccurate compen-

sation. It is only necessary to achieve repeatable shapes which fit within the barrel envelope. Therefore, any of the etch mask patterns presented in Chapter 4 should work. The latest barrel design was shown by mechanical solid modeling construction to be achievable. A specialist in the high volume production of complicated small screw machined parts has been located who is able to fabricate the barrel. The only risk in packaging now is in the bonding interface as previously discussed.

Surface micromachining is a more complicated issue. The very simple piezoresistor sensor shown in Chapter 4 entails very little risk of accomplishment with regard to the micro machining process or CMOS process steps. However, using both metal and poly2 as sacrificial layers limits the circuit design choices in layout geometry. The simple bridge pattern presented is probably inadequately matched or not very well-compensated. For sensitivity and calibration improvements of the piezoresistive sensing bridge design, there is a need to have as much design freedom as possible. The risk that the design problem is overly constrained is low to moderate.

Capacitive sensor approaches require that a metal layer (as capacitor upper plate) be retained after etching. This entails moderate risk for a design that is presumed to be workable but unverified. Many details need to be worked out, but there is a great deal of flexibility in selecting the processes. Given the documented success of $XeF_2$ as an etchant for poly-silicon, there is an excellent chance for this design to succeed. The limiting factor is the ability to open contacts to the poly2 layer with only relatively minor damage to it. It can then be reliably sacrificed by $XeF_2$ etch. If necessary, a capacitor constructed with substrate diffusion as a capacitor bottom plate allows both poly2 and poly1 layers to be sacrificed. The resultant decrease in capacitance and sensitivity may present additional challenge in the electronic design. The risk is low to moderate, however.

### *5.2.2 Electronic Design*

Before the fully integrated MEMS sensor IC electronics design can proceed, the IC subsystem design needs to be fully addressed. The subsystem design includes: allocation of requirements to the functional blocks, the development and tradeoff of candidate circuit implementations, the development of embedded algorithms, including sensor data processing, I/O communication, and self test and calibration. Final development with a breadboard system can use the phase 1 test chips. Adding appropriate hardware and software will provide an initial means of testing and evaluating the subsystem design as it progresses.

Also more work on the integrated electronics design is needed. Several of these functional blocks are complex and intricate, although considered individually do not require technology development to implement. Taken together, they present a significant effort. The integrated design must fit within significant size constraints. Additionally process yield, noise, and long term stability of the integrated design are important factors in this design effort.

The use of licensed designs presents a significant area for design simplification. Licensing high precision circuit designs–including the operational amplifiers, analog to digital converters, and digital processing circuits– should provide a means of reducing non-recurring design costs and risks of the integrated circuit. Additional surveying of designs available from the electronic industry and academia is recommended.

### 5.2.3 Commercialization

RainTree has very high hopes that the San Diego County Air Pollution Control District will provide a funding grant to help implement first production of Sure✔ devices. The proposal was submitted August 5, 1996. The funding amounts are large and results show high potential for achieving their objectives.

# CHAPTER 6

# RECOMMENDATIONS

# 6 Recommendations

RainTree Technology recommends that the work begun in this project be continued in a phase II SBIR. In the intermediate term between this phase and the start of the phase II SBIR, RainTree Technology should continue work on the integration and test of the barrel and IC interface. As a minimum, our near term plans include completing and demonstrating barrel fabrication and integration with anisotropically formed IC "dummies". To the extent possible, plans are to complete fabrication and testing the test items already designed. Addendum or amendment pages to this report will be distributed as results from these near term efforts dictate. Specific tasks and investigations which should be addressed in follow-on work include:

(1) performing further tradeoffs and final selection of piezoresistive versus capacitive sensor designs,

(2) evaluating alternative bonding processes and the effect of new designs on the barrel and integrated circuit interface,

(3) reliability testing of the interface bonding using "dummy chips" from multi-lot wafer samples (to include thickness variation, metal fabrication tolerances, manufacturing/assembly variations.),

(4) determination of process reliability for selected CMOS and surface micro-machining process,

(5) determination of self-test and recalibration methods to ensure acceptability, reliability, and safety of the product, and

(6) completing all integrated circuit development steps as presented in chapter 5.

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# APPENDIX A

## Structural Analysis of Silicon Integrated Circuit and Novel Package

DERIAN CONSULTING

Structural Design, Analysis & Optimization Mechanism Design, Analysis & Optimization

Thursday, June 13, 1996

# Structural Analysis of Silicon Integrated Circuit and Novel Package

for

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# DERIAN CONSULTING

Structural Design, Analysis & Optimization Mechanism Design, Analysis & Optimization

## INTRODUCTION:

The Mechanical behavior of a Silicon Integrated Circuit and Novel package was simulated using Pro/Mechanica FEA Software. The structure was subjected to Thermal and Pressure loading. Four separate load cases were analyzed. A strength analysis of the IC, Barrel (package) and Bond line interfaces were performed. The mechanical response of the Silicon Membrane was analyzed.

## FINITE ELEMENT MODEL:

The model was derived from Dimensioned drawings and DXF data files provided by RainTree (Figure 1). The Pro/Mechanica Software package was used to create and solve the Finite Element Model. The model used in the analysis is illustrated in Figure 2. Because the model is symmetric, only half of the structure was modeled. The 2-D geometry was imported into Mechanica. A 3-D wire framed was built and then 112 solid elements were created to map the geometry. The Model consists of three major parts: 1) The BARREL consists of a metal (kovar) tube containing a slit. The barrel to the right of the slit is depressed forming a window and a shelf. 2) The IC (silicon)is located through the window and it interfaces both on the inside of the barrel and the outside of the barrel on the shelf. The exposed portion of the IC has features defining a thin membrane over a evacuated chamber (Figure 3). 3)The BOND LINES (epoxy) are modeled as .025 mm (.001") thick. These elements connect the IC to the barrel.

Table 1 list the properties for the different materials used in the model.

Four load cases were analyzed. The loading conditions are given below.

| | PRESSURE | TEMPERATURE |
|---|---|---|
| **CASE 1** | 0.000 $N/mm^2$ | 25° C |
| **CASE 2** | 5.512 $N/mm^2$ | 25° C |
| **CASE 3** | 5.512 $N/mm^2$ | 200° C |
| **CASE 4** | 5.512 $N/mm^2$ | -55° C |

For all analyses the stress free temperature was set to 150°C, the cure temperature of the epoxy bond lines. The pressure load was applied to all external surfaces. The temperatures were applied uniformly over the whole model.

Constraints were applied to the model in a cylindrical coordinate system. The plane of symmetry was constrained in the tangential direction. The large end was constrained in the radial direction and the small end was constrained in the radial and axial direction.

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## STRENGTH ANALYSIS

The strength analysis for the four load cases are summarized and presented in Table 2. The Margin of safety reported in Table 2 is calculated by the following formula

$$\text{Margin of Safety} = \frac{(\text{Factor of safety})*(\text{Allowable stress})}{\text{Maximum stress}} - 1$$

For the Kovar and Silicon the factor of safety used was 1.2. Because of the uncertainty inherent in adhesive bond line stresses the factor of safety used there was 1.4. Using this method of strength criteria the margin of safety must be greater than zero

In Table 2 it is evident that for each region of the model, the highest stress is observed in Load Case 4. Load cases 2-4 are all subjected to the same 5.5 $N/mm^2$ pressure load. But case 4 has the largest temperature load [150°C - (-55°C) = 205°C]. Therefore most of the following stress result discussions will be limited to case 4.

The radial and axial displacement fields for case 4 are shown in Figures 4 & 5. In Figure 4 it is shown that the greatest radial displacement is in the shelf region. Notice the "S" shape bending in the IC. In a cross sectional view, the shelf is flat. However, the barrel surface is round. Just as curved beams are stiffer than straight beams, the barrel is stiffer than the flat shelf. Loads follow the stiffest path. Therefore the pressure loads on the free end of the shelf flow through the IC and the two bond lines to the barrel. This load path through the bond lines gives rise to high bond line stresses which will be discussed later in this section. Figure 5 shows the axial displacements. The -55°C temperature load shrinks the model towards the right fixed end of the barrel. Note the non uniform displacement field at the barrel slit due the element rotations in the plane of the page

Figure 6 shows the Von Mises stresses on the Kovar barrel. The Von Mises stress is a Failure Criteria suitable for the ductile materials such as Kovar. When the Von Mises stress equals the allowable stress, yielding occurs. The maximum stress is 180 Mpa and the Margin of Safety (MoS) = 0.6. Because the peak stress is very localized and the Kovar is a ductile material, local yielding could occur with out causing catastrophic failure. Additionally in the model, the geometry is represented by sharp corners. In the real part these regions will be filleted. Filleted corners have reduced stress concentrations than sharp ones.

Figure 7 shows the Minimum principal (maximum compression) stress in the IC. Max Principle stress is a suitable failure criteria for the brittle silicon. A maximum value of 63.2 Mpa (MoS=8.23) is reported in the corner of the membrane cavity. Because the cavity walls are formed by etching , not

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## MEMBRANE ANALYSIS

Analyses were performed to characterize the mechanical response of the pressure sensing membrane as the temperature load is varied. Three different membrane configurations were analyzed under the load cases defined above. For each a different quantity was investigated. No special conclusion was sought from the collective. Refer to Figure 1 for the general membrane geometry

| *MEMBRANE DIMENSIONS (mm)* | *MEASURED QUANTITY* |
|---|---|
| 1. .200 X .200 X .030 | max. stress vs. temp |
| 2. .200 X .200 X .005 | max. displacement vs. temp |
| 3. .100 X .100 X .005 | stress fringe plot |

Membrane 1 A 30 micron membrane was modeled. The maximum stress at the center of the membrane was measured. Figure 10 shows the relation between the maximum membrane stress and the temperature load for Load Cases 2-4. The horizontal curve gives the membrane stress with no temperature load. Note that the curves cross at the stress free temperature of 150 °C.

Membrane 2 A second analysis was performed on a 5 micron membrane. The displacement of the membrane center, relative to the inside bottom of the cavity was measured. Figure 11 shows the relation between the relative displacement of the membrane center, and the temperature load for Load Cases 2-4. The deformation varies by less than 1% over the temperature range. The horizontal curve gives the membrane stress with no temperature load.

Membrane 3 The 5 micron membrane was reduced in sized by ½ to .1mm X .1mm. Figure 12 shows a color fringe plot of Von Mises stress for the membrane for Load Case 4. The maximum stress is 480 Mpa (MoS=.75). The maximum displacement is .56 microns.

## CONCLUSIONS

The analyses reports high Margins of safety for the Barrel and IC. The structural integrity of these components should be of little concern. However, the margins of safety on the Bond lines are small. Therefore the structural integrity is marginal.

Either design modifications should be made to reduce these bond line stresses or a more thorough investigation of the bond line should be performed

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machining, the single crystal strength of 700 Mpa is used. For this part both the model and the real part have sharp corners.

Two failure modes are analyzed for the bond lines. 1)Shear Failure, 2)Tensile Failure. Shearing stresses deform solids by rotating elemental volumes. Tensile and compressive stresses deform solids by extending or shortening volumes edges.

Figure 8 shows the two components of Shear stresses on the top & bottom bond lines. The two Shear stress components were vector summed and reported in Table 2. A peak stress of 6.4 Mpa (MoS=.21) is reported for the top bond line.

Figure 9 shows the flat wise (normal to the bond surface) tensile loads on the bond line. A peak value of 16.9 Mpa (MoS=.02) is reported. These stresses are cause by at least two factors.

- The epoxy adhesive has a much larger CTE. than the barrel or IC. At -55°C the bond line thickness shrinks relative to the barrel and IC. Because the IC is bonded on both surfaces, both bond lines are put in Tension.
- The shelf is a compliant portion of the structure. The pressure loads on the shelf are transferred to the barrel through the IC, putting the bond line in tension.

Although a positive safety margin is reported here, these relatively high bond line stresses are a cause of some concern for several reasons. 1) As reported in Table 1 the stress allowable values for the bond lines are only estimates. Epoxy bond strengths are dependent on many factors, such as temperature, surface preparation, surface chemistry and processing. 2) The Failure criteria used does not consider the combined Shearing and tensile stresses and the nonlinear nature of bond line stresses. To operate at these small MoS a more sophisticated bond line Analysis should be used, and component testing performed.

## RECOMMENDATIONS

1. Increase the stiffness of the shelf portion of the barrel. This could be accomplished in several ways.
    - Increase the material thickness of the shelf
    - Change the geometry of the shelf. Limit the flat area of the shelf to the region immediately under the IC. Fillet and curve the shelf surface as it transitions into the barrel.
    - Minimized the window opening to that just big enough for the IC. This additional material could stiffen the shelf.
2. Explore alternate configurations which would have only one interface surface between the IC and the Barrel. In the current configuration the parallelism, flatness and separation on the two bonding surfaces of the barrel need all to be tightly controlled. In a single interface configuration only the flatness needs to be controlled. Secondly this would eliminate the bending in the IC and stresses on the Bond line.

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# MATERIAL PROPERRTIES

| | MATERIALS | | |
|---|---|---|---|
| PROPERTY | KOVAR | SILICON | EPOXY |
| COEFFICIENT OF THERMAL EXPANSION ( $1^{-6}$ $C^{-1}$ ) | 2.30 | 2.30 | 28.00 |
| YOUNG'S MODULUS $N/mm^2$ (Mpa) | 1.38E+05 | 1.90E+05 | 2.70E+03 |
| STRESS ALLOWABLE $N/mm^2$(Mpa) | 345 | 700 | 24.15 |
| SHEAR STRESS ALLOWABLE $N/mm^2$(Mpa) | | | 13.8 |
| SOURCE | (1) | (2) | (3) |

(1) Vender Data
(2) Kurt Petersen, Silicon as a Mechanical Material
(3) Engineering Estimate

**TABLE 1**

# NOVEL PACKAGE IC
## STRENGTH ANALYSIS

| STRESS (MPa) | LOAD CASE 1<br>25 'C<br>0 PSI | LOAD CASE 2<br>25 'C<br>800 PSI | LOAD CASE 3<br>200 'C<br>800 PSI | LOAD CASE 4<br>-55 'C<br>800 PSI | ALLOWABLE (Mpa) |
|---|---|---|---|---|---|
| **KOVAR CASE** | | | | | |
| Von Mises Stress | 24 | 178 | 165 | 180 | 345 |
| *Margin Of Safety (1)* | **10.98** | **0.62** | **0.74** | **0.60** | |
| **SILICON IC** | | | | | |
| Max Prin Stress | 8.0 | 62.3 | 60.5 | 63.2 | 700 |
| *Margin Of Safety (1)* | **71.92** | **8.36** | **8.64** | **8.23** | |
| **TOP BOND LINE** | | | | | |
| Max Shear Stress | 0.5 | 4.5 | 3.7 | 6.1 | 10.35 |
| *Margin Of Safety (2)* | **12.73** | **0.66** | **1.00** | **0.21** | |
| Flat Wise Tension | 0.8 | 4.2 | 4.5 | 6.0 | 24.2 |
| *Margin Of Safety (2)* | **22.05** | **3.12** | **2.84** | **1.88** | |
| **BOT. BOND LINE** | | | | | |
| Max Shear Stress | 2.48 | 3.46 | 2.55 | 5.11 | 10.35 |
| *Margin Of Safety (2)* | **1.98** | **1.14** | **1.90** | **0.45** | |
| Flat Wise Tension | 2.70 | 12.6 | 9.6 | 16.89 | 24.2 |
| *Margin Of Safety (2)* | **5.40** | **0.37** | **0.80** | **0.02** | |

*(1) Factor of Saftey = 1.2*
*(2) Factor of Saftey = 1.4*

**TABLE 2**

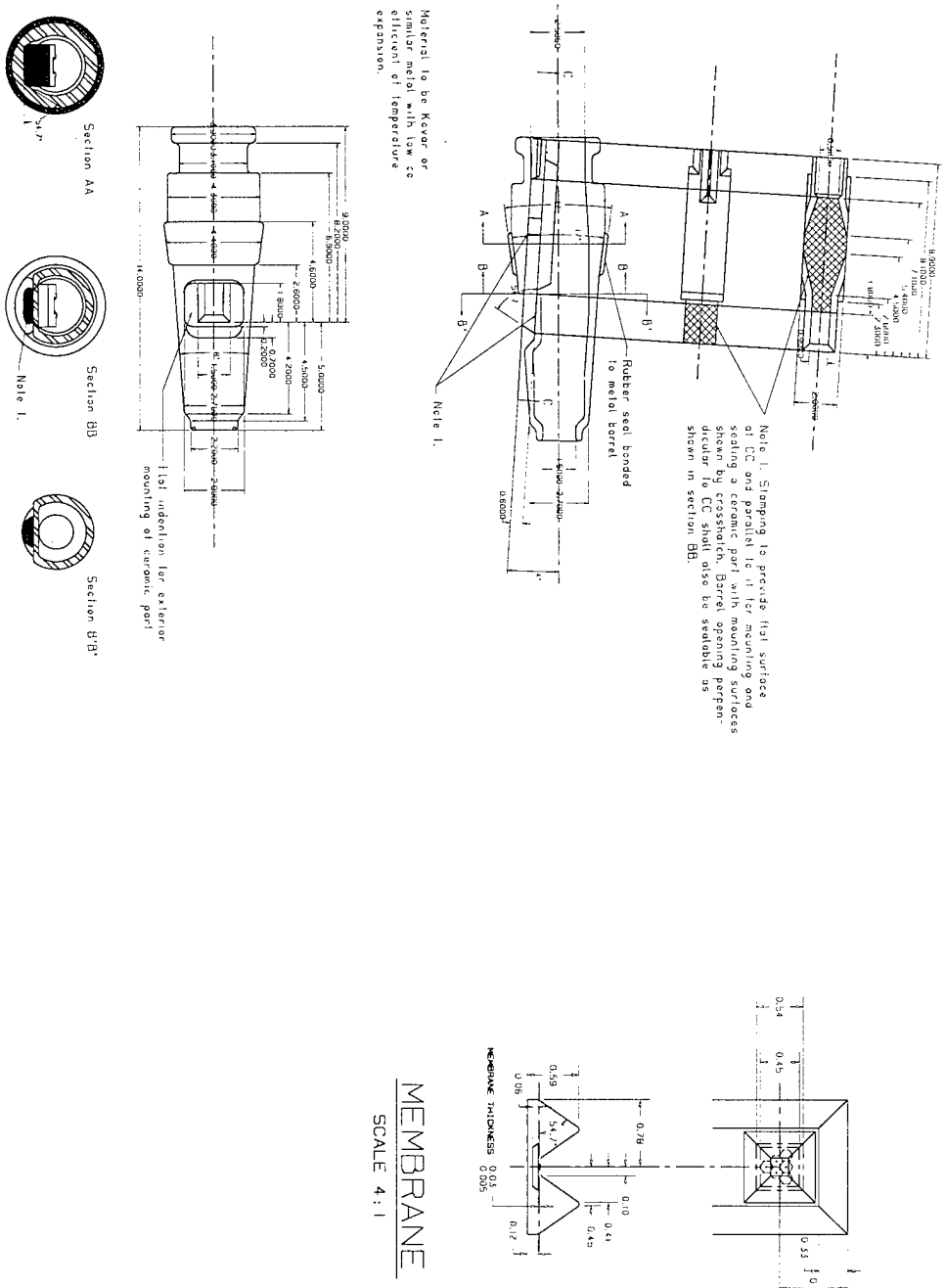
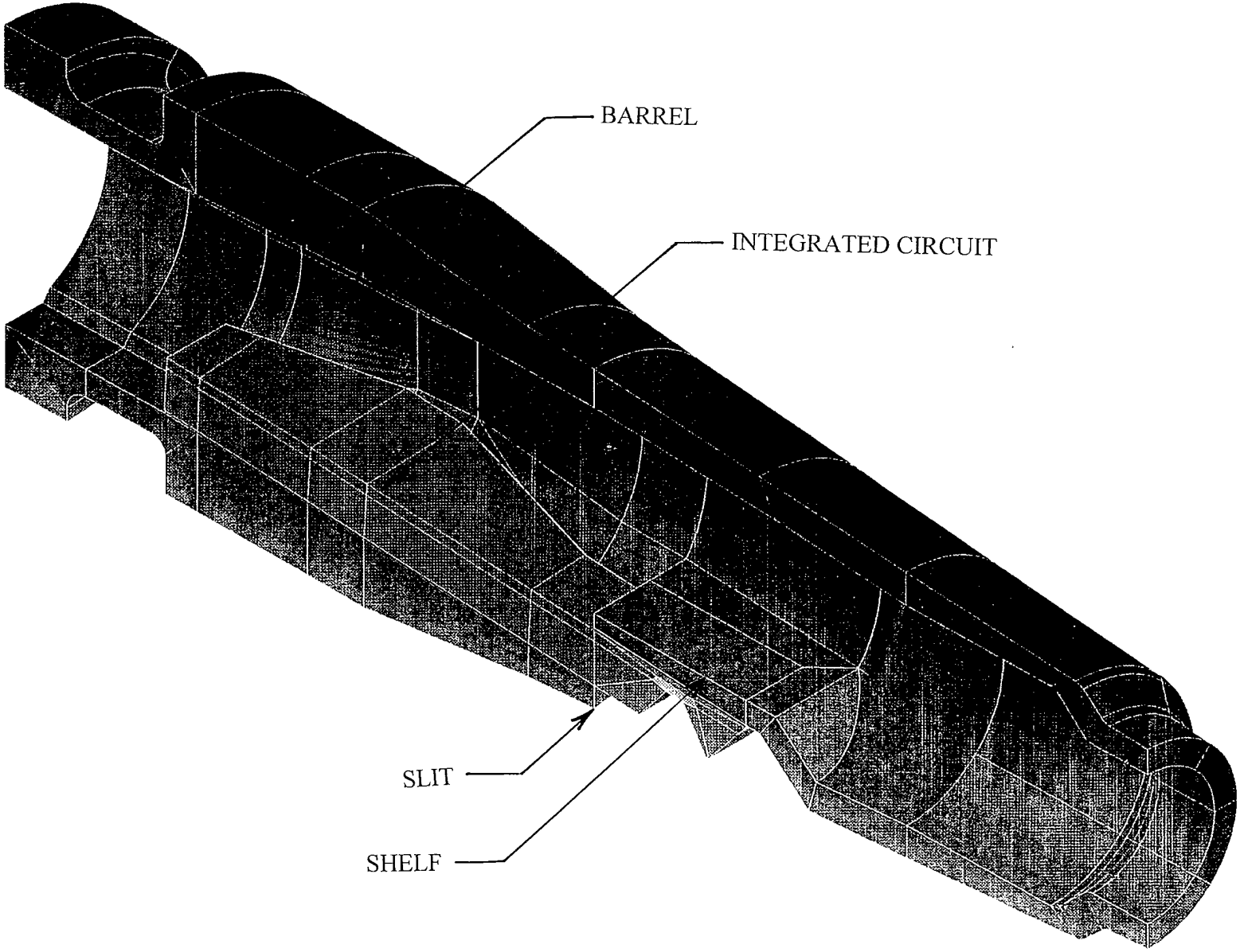



FIGURE 1 REFERENCE GEOMETRY

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IC and Novel Package

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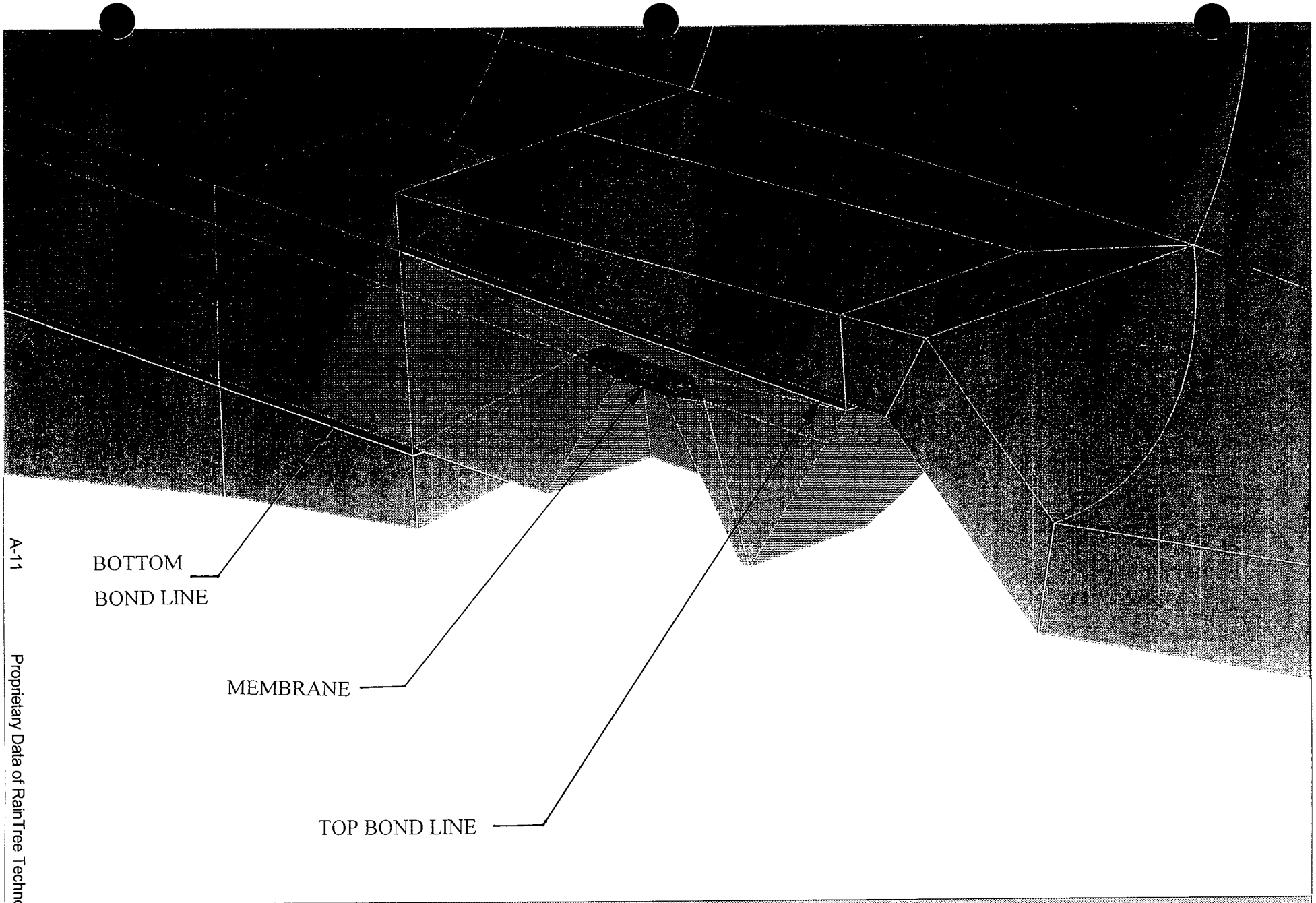

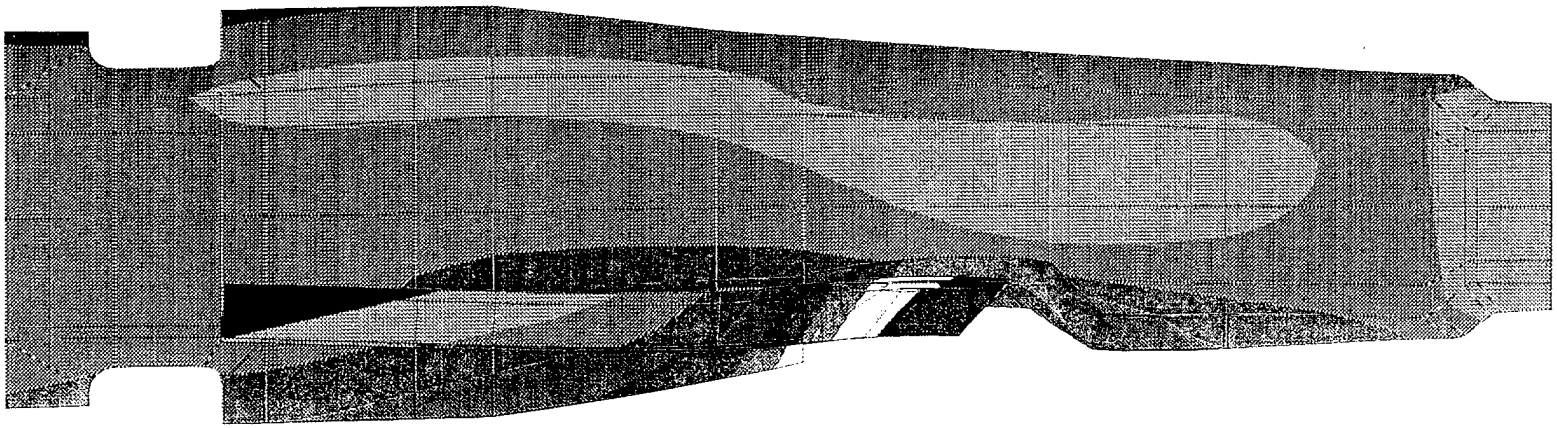

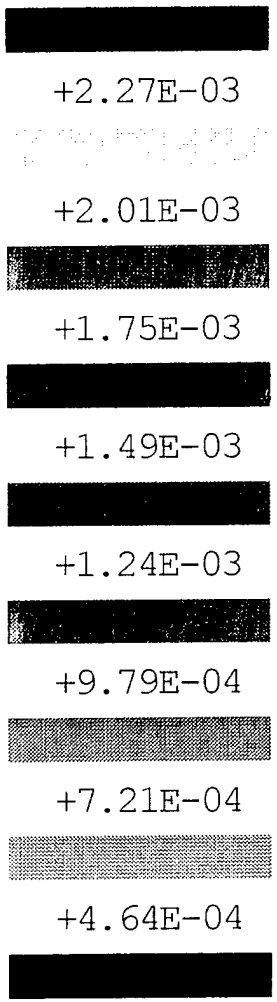


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Radial Displacement 800 psi, -55C

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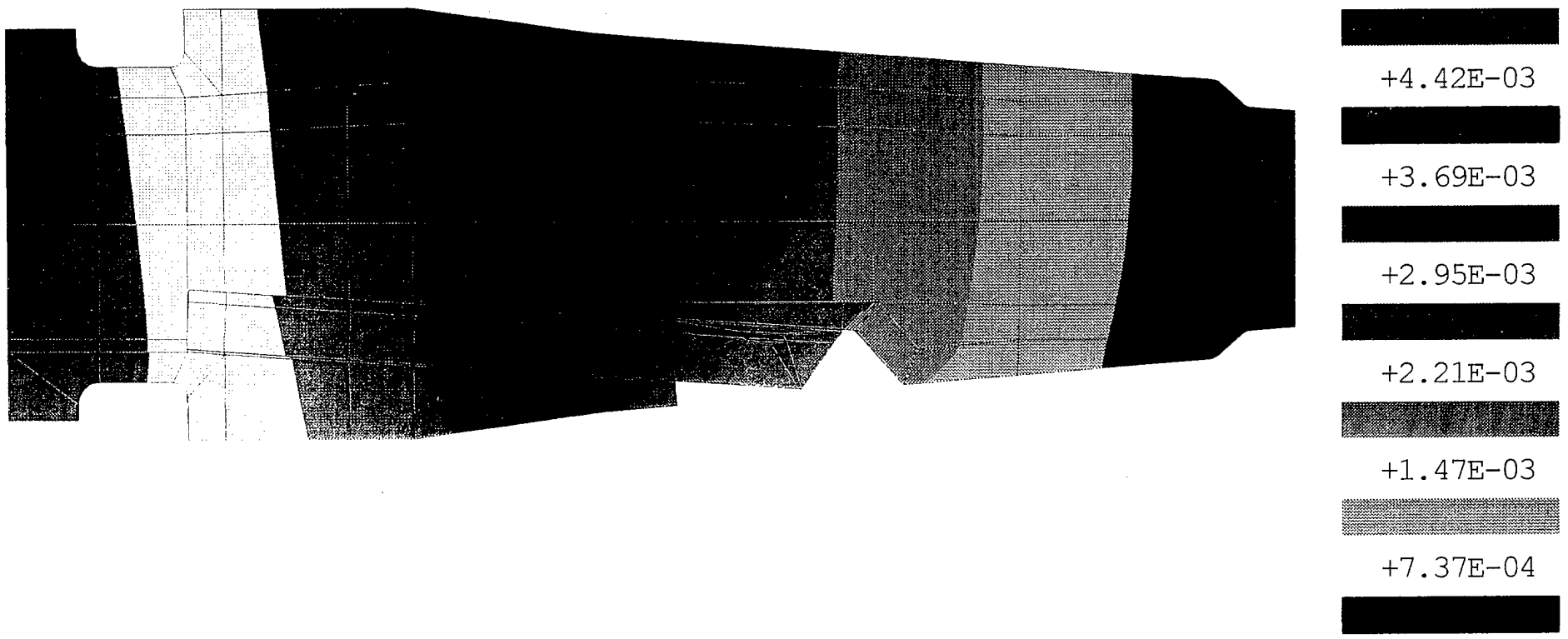


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Axial Displacement 800 psi, -55C

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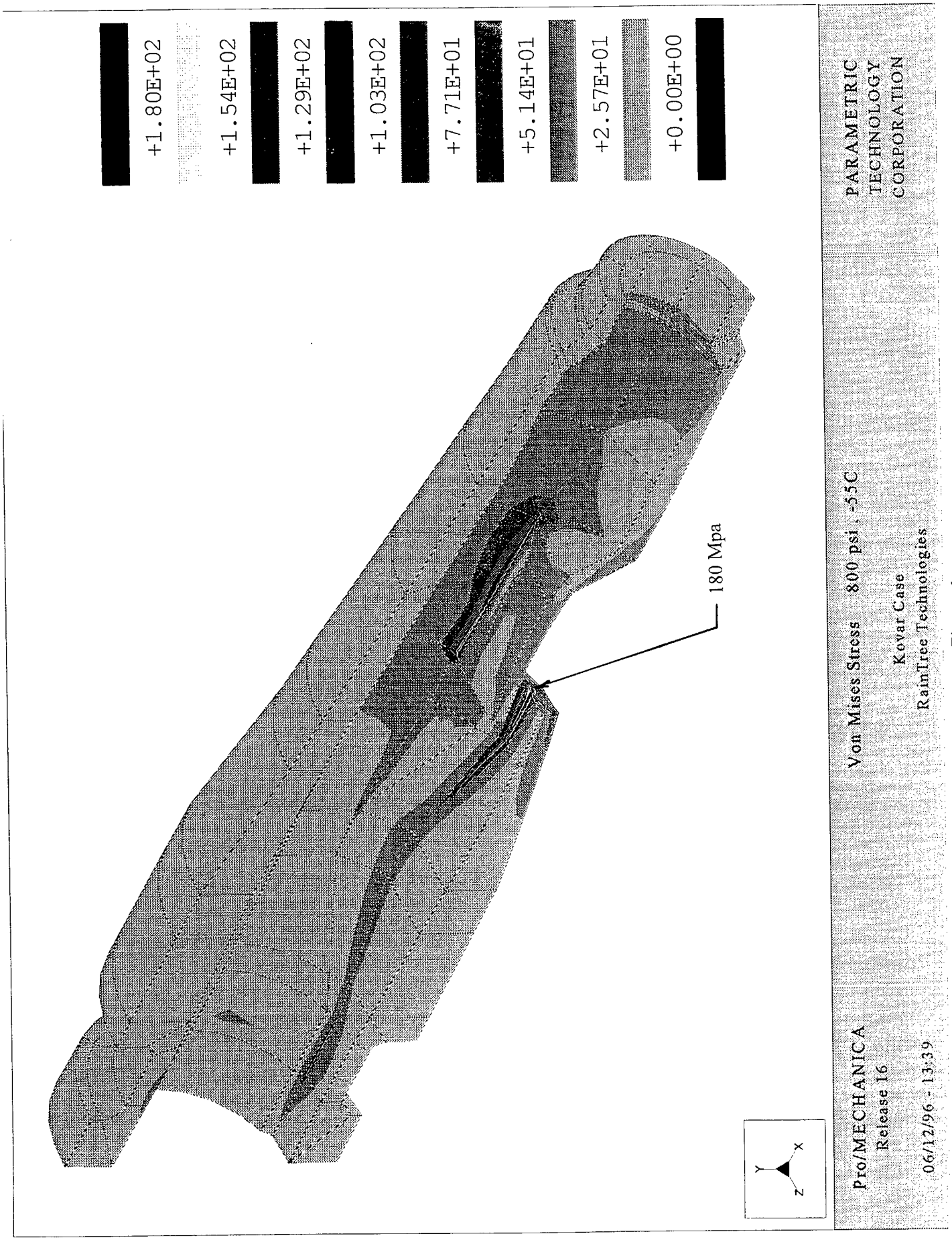
Figure 5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Von Mises Stress 800 psi, -55C
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Figure 6

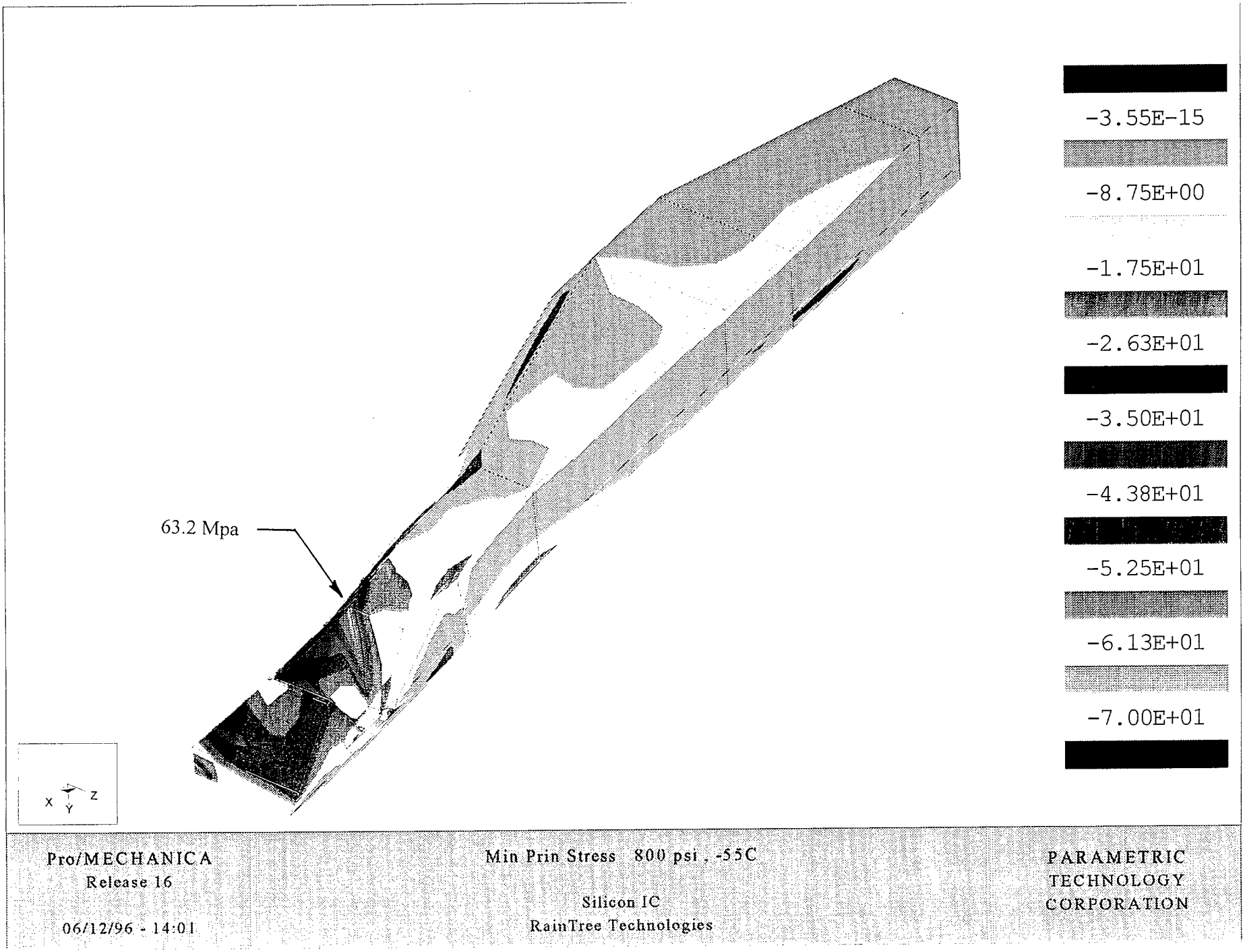


Figure 7

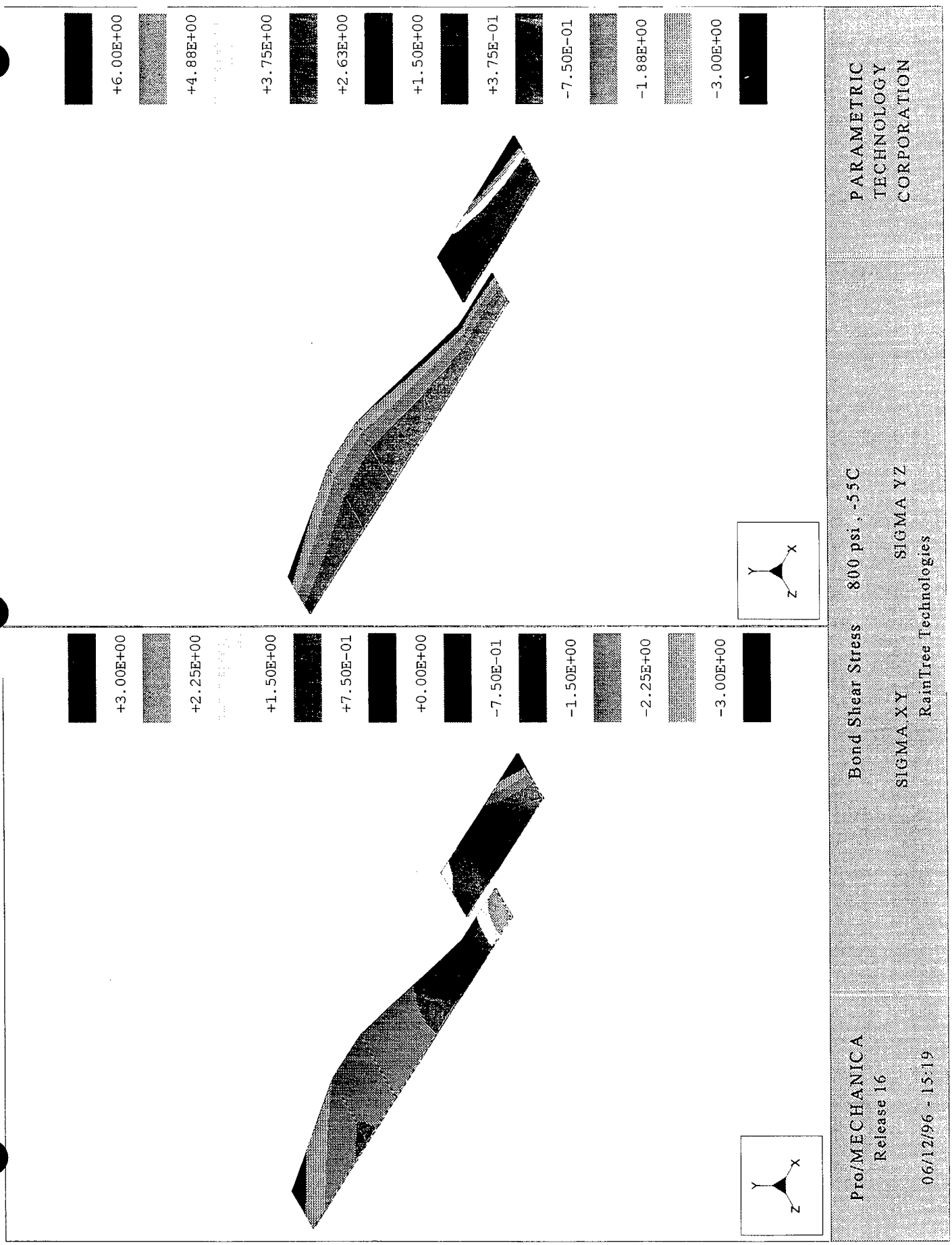
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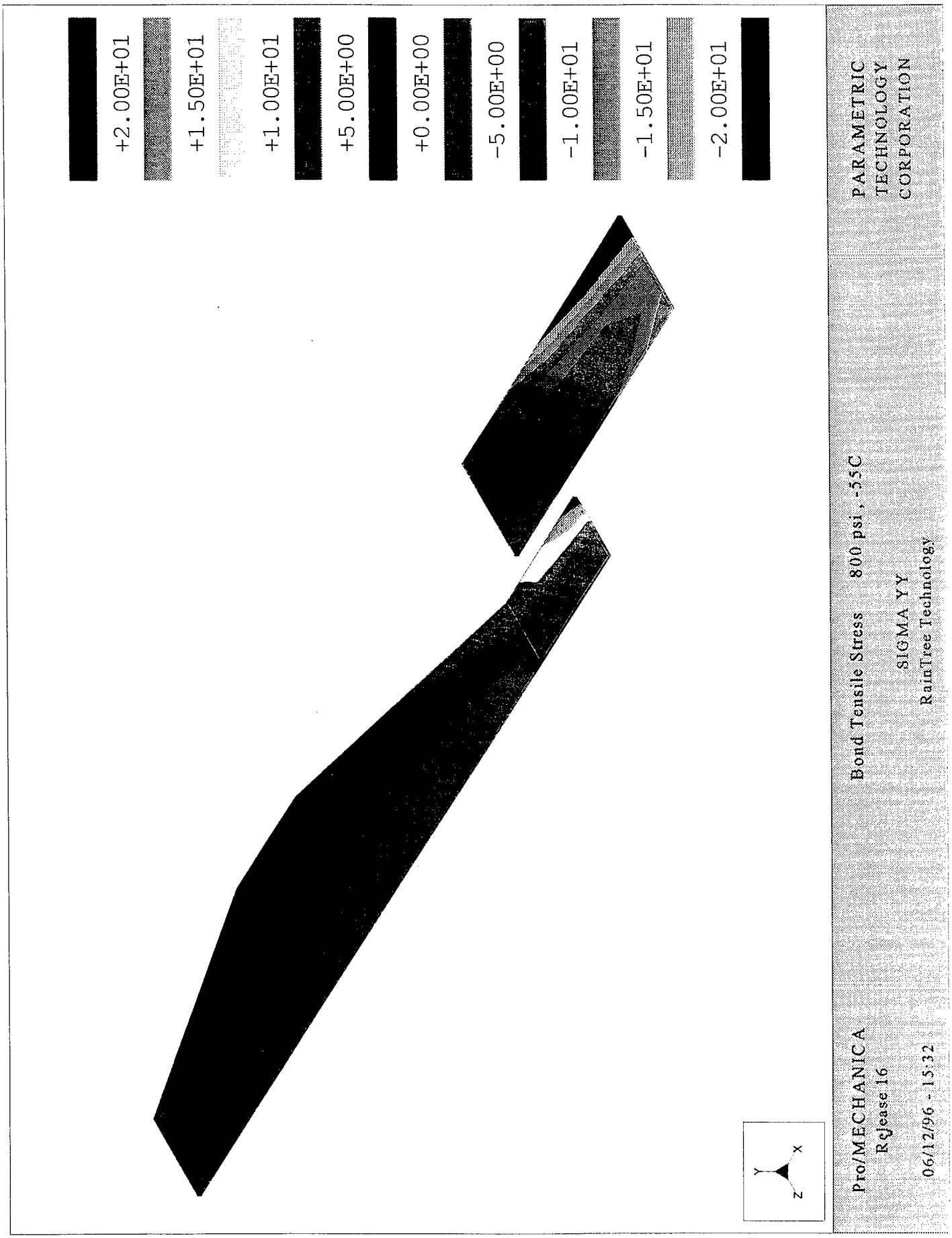
Figure 8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-1.00E+01
-1.50E+01
-2.00E+01
PARAMETRIC TECHNOLOGY CORPORATION
Bond Tensile Stress 800 psi, -55C
SIGMA YY
RainTree Technology
Pro/MECHANICA
Release 16
06/12/96 - 15:32
X
Y
Z

Figure 9

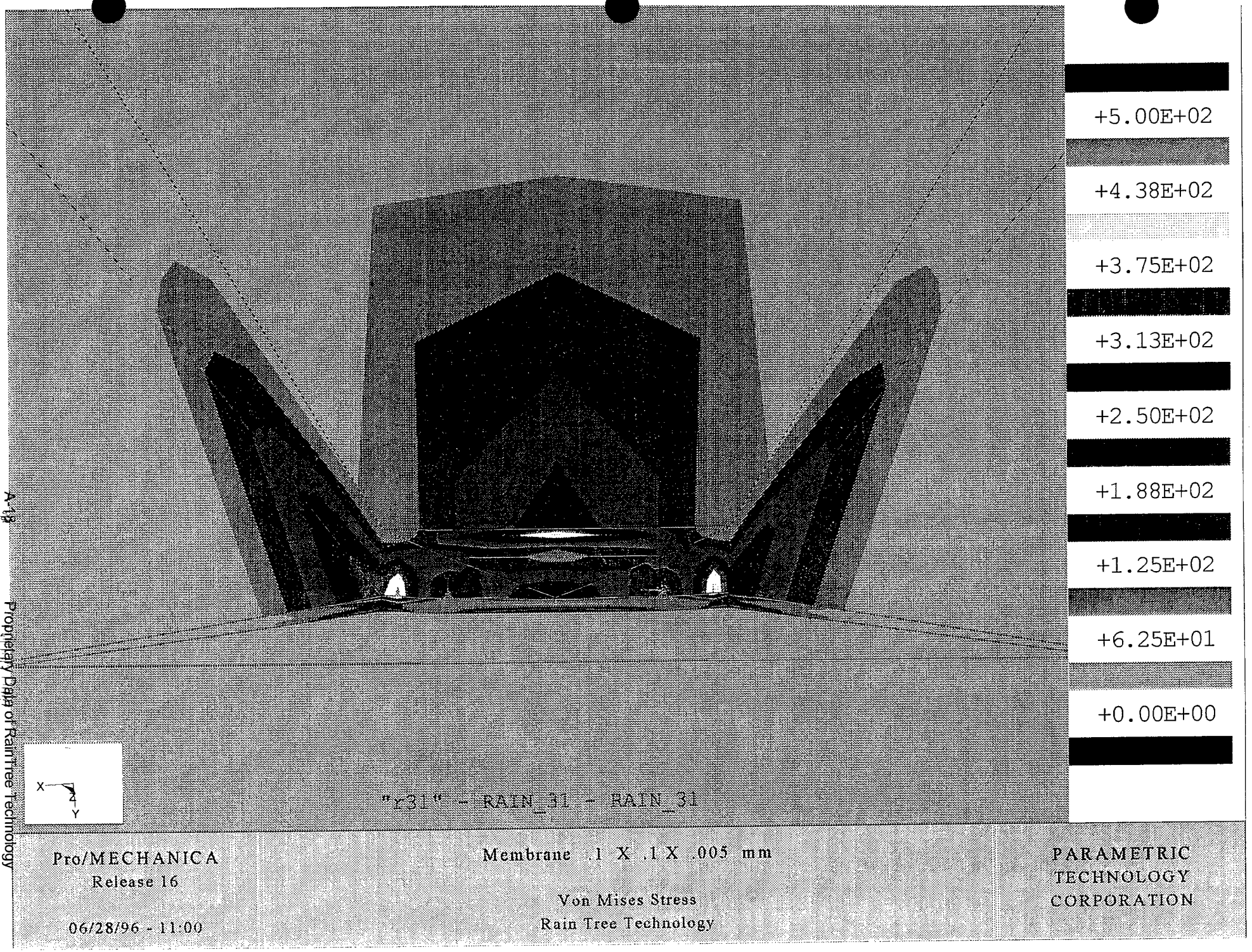


Figure 12

DERIAN CONSULTING

Structural Design, Analysis & Optimization Mechanism Design, Analysis & Optimization

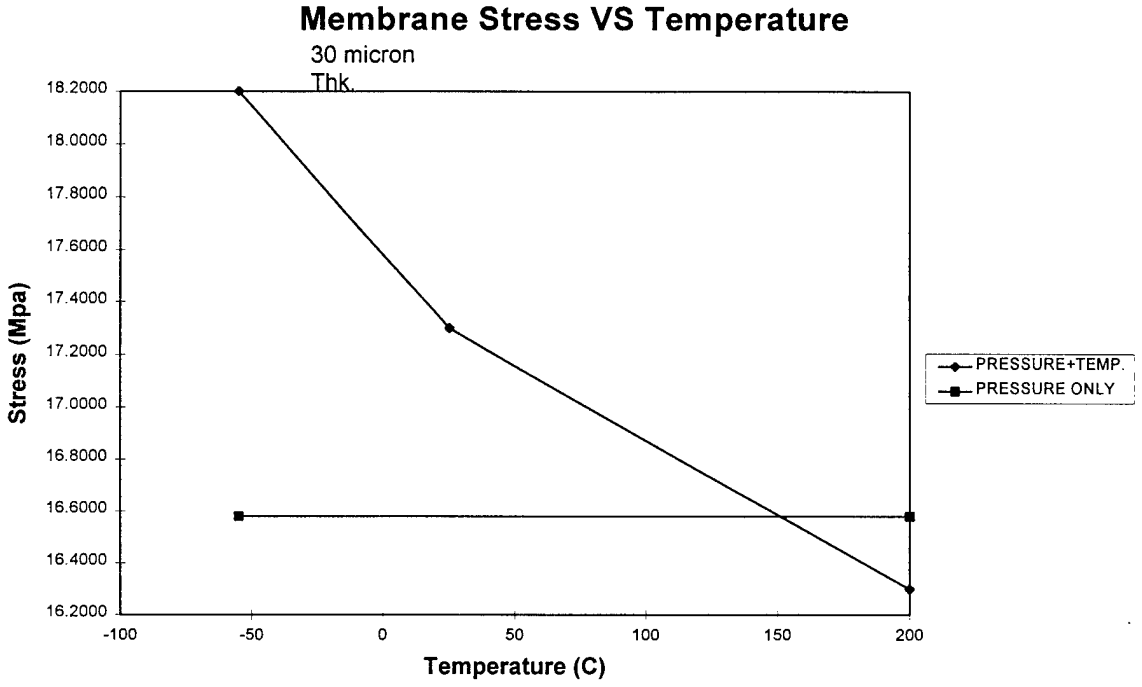


Figure 10

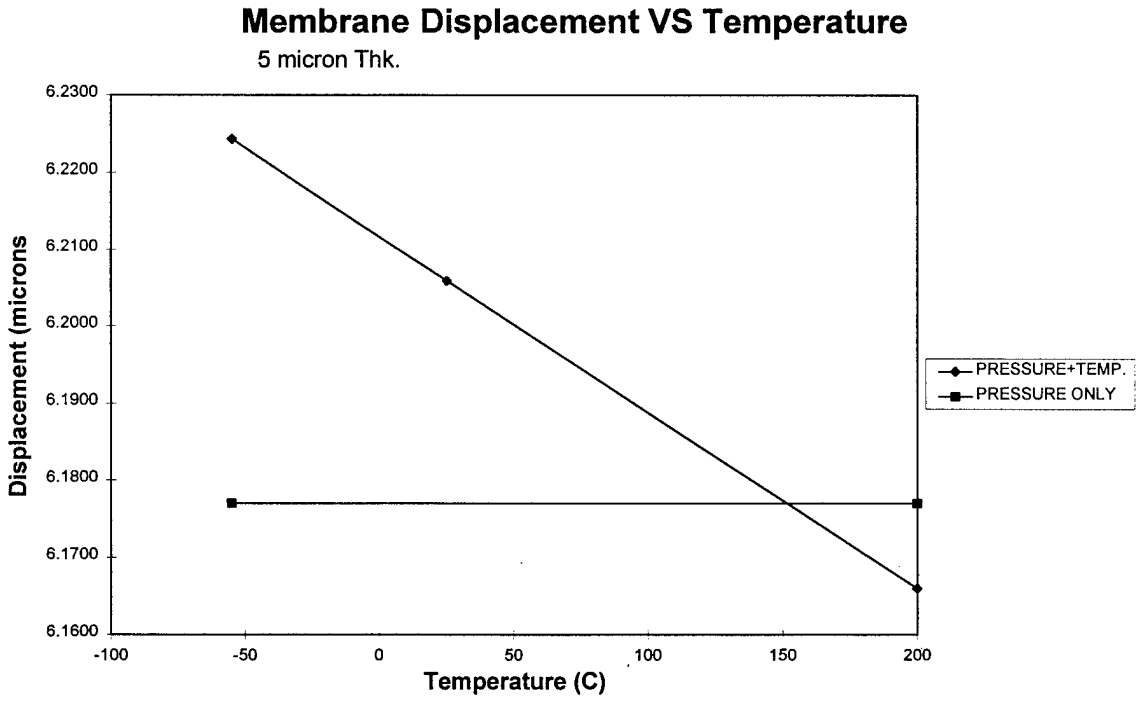


Figure 11

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# APPENDIX B

## T-SPICE SIMULATION LISTINGS

# Appendix B: TSPICE Simulation Listings

This appendix includes the following simulation files for reference. These files were used to generate the test chip operating plots included in Chapter-4.

| Filename | Description |
|---|---|
| a60244f.sp | TSPICE Simulation listing for operation of the test chip for integrated bridge capacitance measurement with .0244 pF (~25 psia) variable (pressure dependent) capacitance and 2 pF fixed and reference capacitance. |
| fc1.sp | TSPICE Simulation listing for operation of the test chip for charge redistribution capacitance measurement with .244 pF (~250 psia) variable (pressure dependent) capacitance and 2 pF fixed and reference capacitance. |
| a70244.sp | TSPICE Simulation listing for operation of the test chip for integrated bridge capacitance measurement using the internal feedback capacitor with .0244 pF (~25 psia) variable (pressure dependent) capacitance and 2 pF fixed and reference capacitance. |
| rttchipx.ckt | TSPICE subcircuit listing for test chip. |
| rttchipx.ckt | TSPICE subcircuit listing for test chip. |
| iopad.ckt | TSPICE subcircuit listing for iopad macrocell. |
| bpad.ckt | TSPICE subcircuit listing for bare pad (no clamping transistors) macrocell. |
| ppad.ckt | TSPICE subcircuit listing for power pad (used for VCC and GND) macrocell. |
| tgate.ckt | TSPICE subcircuit listing for transmission gate macrocell. |
| startup.ckt | TSPICE subcircuit listing for startup circuit macrocell. |
| biasgen.ckt | TSPICE subcircuit listing for bias generator macrocell. |
| biassplt.ckt | TSPICE subcircuit listing for bias splitter macrocell. |
| amp.ckt | TSPICE subcircuit listing for op amp and comparator macrocell. |
| j2nwell.md | Level 2 SPICE MOSFET parameters for Orbit, 2 micron n-well process. |
| rttchip.lib | TSPICE library listing for all macrocells used in test chip simulations. |

```
* TEST CHIP BRIDGE GAIN CIRCUIT          Revised:    August 16, 1996
*                    Revision: 00
* RAIN TREE TECHNOLOGY
*
* This circuit tests the operation of the test chip as an integrated capacitance bridge
*
X1 VREF  VFDBK VFDBK VC0 VC1 VC2 VC3 VC4 VC5 VC6 VC7 VOUT  DOUT  VCC GND  RTTCHIPX
*
*  CREF  (VREF, GND)
VC0 VC0 0 BIT ({ 0 9(0) 1 50(01)} PW=50U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
VC1 VC1 0 BIT ({ 0 9(1) 1 50(10)} PW=50U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
*  CSENSE (VREF, GND)
VC2 VC2 0 BIT ({ 0 9(1) 1 50(10)} PW=50U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
VC3 VC3 0 BIT ({ 0 9(0) 1 50(01)} PW=50U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
*  COMMON (VFDBK, GND)
VC4 VC4 0 BIT ({ 0 9(0) 1 50(01)} PW=50U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
VC5 VC5 0 BIT ({ 0 9(1) 1 50(11)} PW=50U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
*  FDBK   (VFDBK, GND)
VC6 VC6 0 BIT ({ 0 9(0) 1 50(01)} PW=50U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
VC7 VC7 0 BIT ({ 0 9(1) 1 50(11)} PW=50U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
*
*  POWER SUPPLIES
*
VCC VCC 0 PWL(0 0 1U 5 1 5)
VREF VREF 0 PWL(0 0 1U 5 1 5)
VFDBK VFDBK 0 PWL(0 0 1U 2.5 1 2.5)
*
*  EXTERNAL COMPONENTS
*
CVOUT VOUT 0 50PF
CDOUT DOUT 0 50PF
*
*RVOUT VOUT 0 10MEG
*RDOUT DOUT 0 10MEG
*
.TRAN 1U 1000U
.PRINT TRAN  VOUT
.LIB RTTCHIP.LIB
.END
```

---

LASTREF.TXT

```
* TEST CHIP REDISTRIBUTION FREQ RANGE CIRCUIT          Revised:    August 16, 1996
*                    Revision: 00
* RAIN TREE TECHNOLOGY
*
* This circuit tests the operation of the test chip as a charge redistribution capacitance measurement
*
X1 VREF  VFDBK VFDBK VC0 VC1 VC2 VC3 VC4 VC5 VC6 VC7 VOUT  DOUT  VCC GND  RTTCHIPX
*
*  CREF  (VCC, GND)
VC0 VC0 0 BIT ({ 0 0 50(1)} PW=500U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
```

```
VC1 VC1 0 BIT ({ 0 1 50(0)} PW=500U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
*  CSENSE (VCC, GND)
VC2 VC2 0 BIT ({ 0 1 50(0)} PW=500U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
VC3 VC3 0 BIT ({ 0 0 50(1)} PW=500U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
*  COMMON (DOUT, GND)
VC4 VC4 0 BIT ({ 0 0 50(1)} PW=500U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
VC5 VC5 0 BIT ({ 0 1 50(1)} PW=500U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
*  FDBK   (DOUT, GND)
VC6 VC6 0 BIT ({ 0 0 50(0)} PW=500U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
VC7 VC7 0 BIT ({ 0 1 50(1)} PW=500U ON=5.0 OFF=0.0 RT=2N FT=2N) ROUND=2N
*
*  POWER SUPPLIES
*
VCC VCC 0 PWL(0 0 1U 5 1 5)
VREF VREF 0 PWL(0 0 1U 2.5 1 2.5)
VFDBK VFDBK 0 PWL(0 0 1U 2.5000 1M 2.5000 2M 2.5000 2.001M 1.25 3M 1.25 3.001M .625 4M .625
4.001M .3125 5M .3125 5.001M .15625 6M .15625 6.001M .234375 7M .23475 7.001M .1956875 8M
.1956875 8.001M  .17615625 1 .17615625)
*
*  EXTERNAL COMPONENTS
*
CVOUT VOUT 0 50PF
CDOUT DOUT 0 50PF
*
*RVOUT VOUT 0 10MEG
*RDOUT DOUT 0 10MEG
*
.TRAN 100U 9000U
.PRINT TRAN  DOUT VOUT VFDBK
.LIB RTTCHIP.LIB
.END
```

---

```
* TEST CHIP CIRCUIT              Revised:     August  15, 1996
*                          Revision: 00
* RAIN TREE TECHNOLOGY
*
* This circuit includes the switches, sense capacitors, and op amps for the test chip
*
.SUBCKT RTTCHIPX  VREF  VCOM VFDBK VC0 VC1 VC2 VC3 VC4 VC5 VC6 VC7 VOUT  DOUT  VCC
GND
*              |                  inputs                | outputs | power |
*
*  SWITCH INSTANCES
*
XSW0 VCC CREF VC0 VCC 0 TGATE
XSW1 0   CREF VC1 VCC 0 TGATE
*
XSW2 VCC CSENSE VC2 VCC 0 TGATE
XSW3 0   CSENSE VC3 VCC 0 TGATE
*
```

```
XSW4 VCOM COMMON VC4 VCC 0 TGATE
XSW5 0    COMMON VC5 VCC 0 TGATE
*
XSW6 VFDBK FDBK VC6 VCC 0 TGATE
XSW7 0    FDBK VC7 VCC 0 TGATE
*
* Op Amp Instance
*
XAMP VOUT COMMON VOUT BP BPC BNC BN VCC 0 AMP
*
* Comparator Instance
*
XCMP COMMON VREF DOUT BP BPC BNC BN VCC 0 AMP
*
* Startup Instance
*
XSTART BIASP START VCC 0 STARTUP
*
* Bias Generator Instance
*
XBIAS BIASP BIASN START VCC 0 BIASNC BIASGEN
*
* Bias Splitter Instance
*
XSPLIT BIASN BIASNC BP BPC BNC BN VCC 0 BIASSPLT
*
* Pad Instances
*
XVCC VCC 0 PPAD
XGND 0 0 PPAD
XVREF VREF VCC 0 IOPAD
XVFDBK VFDBK VCC 0 IOPAD
XVC0 VC0 VCC 0 IOPAD
XVC1 VC1 VCC 0 IOPAD
XVC2 VC2 VCC 0 IOPAD
XVC3 VC3 VCC 0 IOPAD
XVC4 VC4 VCC 0 IOPAD
XVC5 VC5 VCC 0 IOPAD
XVC6 VC6 VCC 0 IOPAD
XVC7 VC7 VCC 0 IOPAD
XVOUT VOUT 0 BPAD
XDOUT DOUT 0 BPAD
*
* CAPACITORS
*
CSENSEF CSENSE COMMON 2P
CSENSEV CSENSE COMMON .0244PF
CREFF CREF COMMON 2P
CFDBKF FDBK COMMON .5P
*
* PARASITICS
*
```

```
CSP CSENSE VCC 20PF
CSR CREF VCC 20PF
CFD FDBK VCC 5PF
.ENDS
```

---

```
* TEST CHIP CIRCUIT              Revised:     August 15, 1996
*                          Revision: 00
* RAIN TREE TECHNOLOGY
*
* This circuit includes the switches, sense capacitors, and op amps for the test chip
*
.SUBCKT RTTCHIPF  VREF  VCOM VFDBK VC0 VC1 VC2 VC3 VC4 VC5 VC6 VC7 VOUT  DOUT  VCC
GND
*              |                  inputs                | outputs | power |
*
*  SWITCH INSTANCES
*
XSW0 VREF CREF VC0 VCC 0 TGATE
XSW1 0    CREF VC1 VCC 0 TGATE
*
XSW2 VREF CSENSE VC2 VCC 0 TGATE
XSW3 0    CSENSE VC3 VCC 0 TGATE
*
XSW4 VCOM COMMON VC4 VCC 0 TGATE
XSW5 0    COMMON VC5 VCC 0 TGATE
*
XSW6 VFDBK FDBK VC6 VCC 0 TGATE
XSW7 0    FDBK VC7 VCC 0 TGATE
*
* Op Amp Instance
*
XAMP VOUT COMMON VOUT BP BPC BNC BN VCC 0 AMP
*
* Comparator Instance
*
XCMP COMMON VREF DOUT BP BPC BNC BN VCC 0 AMP
*
* Startup Instance
*
XSTART BIASP START VCC 0 STARTUP
*
* Bias Generator Instance
*
XBIAS BIASP BIASN START VCC 0 BIASNC BIASGEN
*
* Bias Splitter Instance
*
XSPLIT BIASN BIASNC BP BPC BNC BN VCC 0 BIASSPLT
*
* Pad Instances
*
```

```
XVCC VCC 0 PPAD
XGND 0 0 PPAD
XVREF VREF VCC 0 IOPAD
XVFDBK VFDBK VCC 0 IOPAD
XVC0 VC0 VCC 0 IOPAD
XVC1 VC1 VCC 0 IOPAD
XVC2 VC2 VCC 0 IOPAD
XVC3 VC3 VCC 0 IOPAD
XVC4 VC4 VCC 0 IOPAD
XVC5 VC5 VCC 0 IOPAD
XVC6 VC6 VCC 0 IOPAD
XVC7 VC7 VCC 0 IOPAD
XVOUT VOUT 0 BPAD
XDOUT DOUT 0 BPAD
*
*  CAPACITORS
*
CSENSEF CSENSE COMMON 2P
CSENSEV CSENSE COMMON .244PF
CREFF CREF COMMON 2P
CFDBKF FDBK COMMON .2P
*
*  PARASITICS
*
CSP CSENSE VCC 20PF
CSR CREF VCC 20PF
CFD FDBK VCC 2PF
.ENDS
```

---

```
* DIODE GATE CLAMP                Revised:    August 12, 1996
*                              Revision: 00
* RAIN TREE TECHNOLOGY
*
.SUBCKT IOPAD  1   2    3
*           |   |    |
*           I/O VCC   GND
*
*  Clamping MOSFETs
*
M1 2 2 1 2   CMOSP L=50U W=50U
M2 3 3 1 3   CMOSN L=50U W=50U
*
*  Pad Capacitance
*
CPAD 1 3 290fF
.ENDS
```

---

```
* POWER PAD                    Revised:    August 15, 1996
*                              Revision: 00
* RAIN TREE TECHNOLOGY
```

```
*
.SUBCKT PPAD  1   2
*          |  |
*          I/O GND
*
* Pad Capacitance
*
CPAD 1 2 580fF
.ENDS
```

---

```
* TANNER SWITCH CIRCUIT                Revised:    July  18, 1996
*                              Revision: 00
* RAIN TREE TECHNOLOGY
*
.SUBCKT TGATE 1   2   3   4   5
*         |  |   |   |   |
*         A   B   EN\  VCC  GND
*
* Inverter
*
M1 4 3 6 4  CMOSP L=2U W=4U
M2 6 3 5 5  CMOSN L=2U W=4U
*
* P Pass
*
M7 1 3 2 4  CMOSP L=2U W=4U M=2
*
* N Pass
*
M8 1 6 2 5  CMOSN L=2U W=4U M=2
*
* Compensation
*
M3 1 3 1 5  CMOSN L=4U W=2U
M4 2 3 2 5  CMOSN L=4U W=2U
M5 1 6 1 4  CMOSP L=4U W=2U
M6 2 6 2 4  CMOSP L=4U W=2U
.ENDS
```

---

```
* START UP CIRCUIT              Revised:    July  18, 1996
*                         Revision: 00
* RAIN TREE TECHNOLOGY
*
.SUBCKT  STARTUP  1    2     3    4
*             |    |     |    |
*           BIASP  START  VCC   GND
*
* This is a simple starter designed to interface with a bias generator at
* the P channel current bias point and switch off when sufficient current
* flows in the P channel transistors.
```

```
*
* Input P
*
M1 3 1 7 3   CMOSP L=8U W=50U
*
* Current Source P
*
M2 3 5 5 3   CMOSP L=80U W=8U
*
* Input Current Amplifier
*
M4 7 7 4 4   CMOSN L=8U W=8U
M5 6 7 4 4   CMOSN L=8U W=50U
*
* VGS Drop Q
*
M6 5 5 6 4   CMOSN L=8U W=8U
*
* Output Current Mirror
*
M7 6 6 4 4   CMOSN L=8U W=8U
M3 2 6 4 4   CMOSN L=8U W=8U
*
.ENDS
```

---

```
* MODIFIED BIAS CIRCUIT FROM LINCMOSL Revised:     July  18, 1996
*                          Revision: 00
* RAIN TREE TECHNOLOGY
*
.SUBCKT  BIASGEN 1      2      3    4    5    7
*          |     |      |    |    |    |
*
*          BIASP   BIASN   START   VCC   GND   BIASNC
*
* This is a bias generator that uses an internal resistor
* in a source degenerated current mirror.  The original circuit has
* been modified to add cascode biasing to improve PSRR.  The primary
* output is the VGS voltages BN to GND and BP to VCC.
*
* BP Current Mirror Q's
*
M1 4 1 6 4  CMOSP L=8U W=50U
M2 4 1 1 4  CMOSP L=8U W=50U
*
* Cascode P Q's
*
M3 6 3 7 4   CMOSP L=8U W=50U
M4 1 3 3 4   CMOSP L=8U W=50U
*
* Cascode N Q's
*
```

```
M5 7 7 2 5  CMOSN L=8U W=50U
M6 3 7 9 5  CMOSN L=8U W=50U
*
* Degenerated Current Mirror
*
M7 2 2 5 5  CMOSN L=8U W=50U
M8 9 2 8 5  CMOSN L=8U W=50U M=2
R1 8 5 6K
*
* Stabilizing Capacitor
*
C1 3 4 1P
.ENDS
```

---

```
* BIAS SPLIT CIRCUIT FROM LINCMOSL  Revised:    August 13, 1996
* WITH SOME Q SIZE MODS            Revision: 00
* RAIN TREE TECHNOLOGY
*
.SUBCKT BIASSPLT 1   2   3   4   5   6   7   8
*          |   |   |   |   |   |   |   |
*
*          BIASN BIASNC BP  BPC  BNC  BN  VCC  GND
*
* This is a bias splitter which converts the bias gen bias voltage
* to the cascode bias voltages required by the analog output buffer.
*
* BP Current Mirror Q's
*
M1 7 3 3 7  CMOSP L=4U W=40U
M2 7 3 9 7  CMOSP L=4U W=40U
*
* Cascode P's
*
M3 3 4 4 7  CMOSP L=2U W=40U
M7 9 4 5 7  CMOSP L=2U W=40U
*
* Cascode N's
*
M6 5 5 6 8  CMOSN L=2U W=40U
M8 4 2 10 8 CMOSN L=4U W=4U
*
* BN Current Mirror Q's
*
M4 10 1 8 8  CMOSN L=4U W=4U
M5 6 6 8 8  CMOSN L=4U W=40U
.ENDS
```

---

```
* OP AMP SUBCIRCUIT FROM LINCMOSL ANALOG BUFFER  Revised:    July 18, 1996
*                                  Revision: 00
* RAIN TREE TECHNOLOGY
```

```
*
.SUBCKT  AMP  1   2    3    4    5   6   7  8   9
*         |   |    |    |    |   |   |  |   |
*
*         IN-  IN+   OUT   BP   BPC  BNC  BN VCC  GND
*
* This is a single gain stage CMOS op amp which requires cascode N and P biasing.
*
*
* Input Diff Pairs
*
M2 10 2 11 8   CMOSP L=6U W=44U  M=2
M3 10 1 12 8   CMOSP L=6U W=44U  M=2
*
M9  13 2 15 9  CMOSN L=6U W=44U  M=2
M10 14 1 15 9  CMOSN L=6U W=44U  M=2
*
* P Diff Pair Bias
*
M1 8 4 10 8    CMOSP L=4U W=40U
*
* N Diff Pair Bias
*
M11 15 7 9 9   CMOSN L=4U W=40U
*
* P Cascoded Current Mirror
*
M4 8 14 14 8   CMOSP L=4U W=20U
M5 8 14 16 8   CMOSP L=4U W=20U
M6 16 5 11 8   CMOSP L=2U W=20U
*
* N Cascoded Current Mirror
*
M12 12 12 9 9 CMOSN L=4U W=20U
M14 17 12 9 9 CMOSN L=4U W=20U
M13 13 6 17 9 CMOSN L=2U W=20U
*
* Output Current Follower - P
*
M7 8 13 13 8 CMOSP L=4U W=40U
M8 8 13 3 8  CMOSP L=8U W=25U  M=6
*
* Output Current Follower - N
*
M15 11 11 9 9  CMOSN L=4U W=40U
M16 3 11 9 9   CMOSN L=8U W=25U  M=6
.ENDS
```

---

```
* N61B SPICE LEVEL2 PARAMETERS

.MODEL CMOSN NMOS LEVEL=2 PHI=0.700000 TOX=3.9800E-08 XJ=0.200000U TPG=1
```

```
+ VTO=0.7794 DELTA=3.1470E+00 LD=1.8480E-07 KP=5.9259E-05
+ UO=683.0 UEXP=9.8530E-02 UCRIT=8.4200E+03 RSH=9.5900E+00
+ GAMMA=0.6033 NSUB=8.2550E+15 NFS=9.1000E+10 VMAX=5.1700E+04
+ LAMBDA=3.4430E-02 CGDO=2.4051E-10 CGSO=2.4051E-10
+ CGBO=3.4582E-10 CJ=1.24E-04 MJ=0.828 CJSW=5.68E-10
+ MJSW=0.324 PB=0.66
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0000E-09


.MODEL CMOSP PMOS LEVEL=2 PHI=0.700000 TOX=3.9800E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9373 DELTA=2.9690E+00 LD=1.5620E-07 KP=1.7153E-05
+ UO=197.7 UEXP=2.5700E-01 UCRIT=1.0910E+05 RSH=9.8190E-02
+ GAMMA=0.6667 NSUB=1.0080E+16 NFS=1.1000E+11 VMAX=9.9990E+05
+ LAMBDA=4.2200E-02 CGDO=2.0328E-10 CGSO=2.0328E-10
+ CGBO=4.1603E-10 CJ=3.38E-04 MJ=0.575 CJSW=2.48E-10
+ MJSW=0.289 PB=0.90
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.2980E-07
```

---

```
* Rain Tree Technology Test Chip TSPICE
Master Library File
*                    Last Revision  8/12/96
*
* RTTCHIP.lib
*
.lib j2nwell.md
*                                          *
* Top Level Circuit                        * Pad Circuits
*                                          *
.lib testchip.ckt                          .lib iopad.ckt
.lib simpchip.ckt                          .lib bpad.ckt
.lib rttchip.ckt                           .lib ppad.ckt
.lib rttnchip.ckt
.lib rttchipf.ckt
.lib rttchipx.ckt
.lib rttchpxs.ckt
*
* Analog Circuits
*
.lib startup.ckt
.lib biasgen.ckt
.lib biassplt.ckt
.lib amp.ckt
.lib dualamp.ckt
.lib ndamp.ckt
.lib iopad.ckt
*
* Switch Circuits
*
.lib aswitch.ckt
.lib tgate.ckt
```